SYSTEM

User Guide

PC5-LARGO • CompactPCI® PlusIO CPU Card

5th Generation Intel® Core™ Processor (Broadwell)

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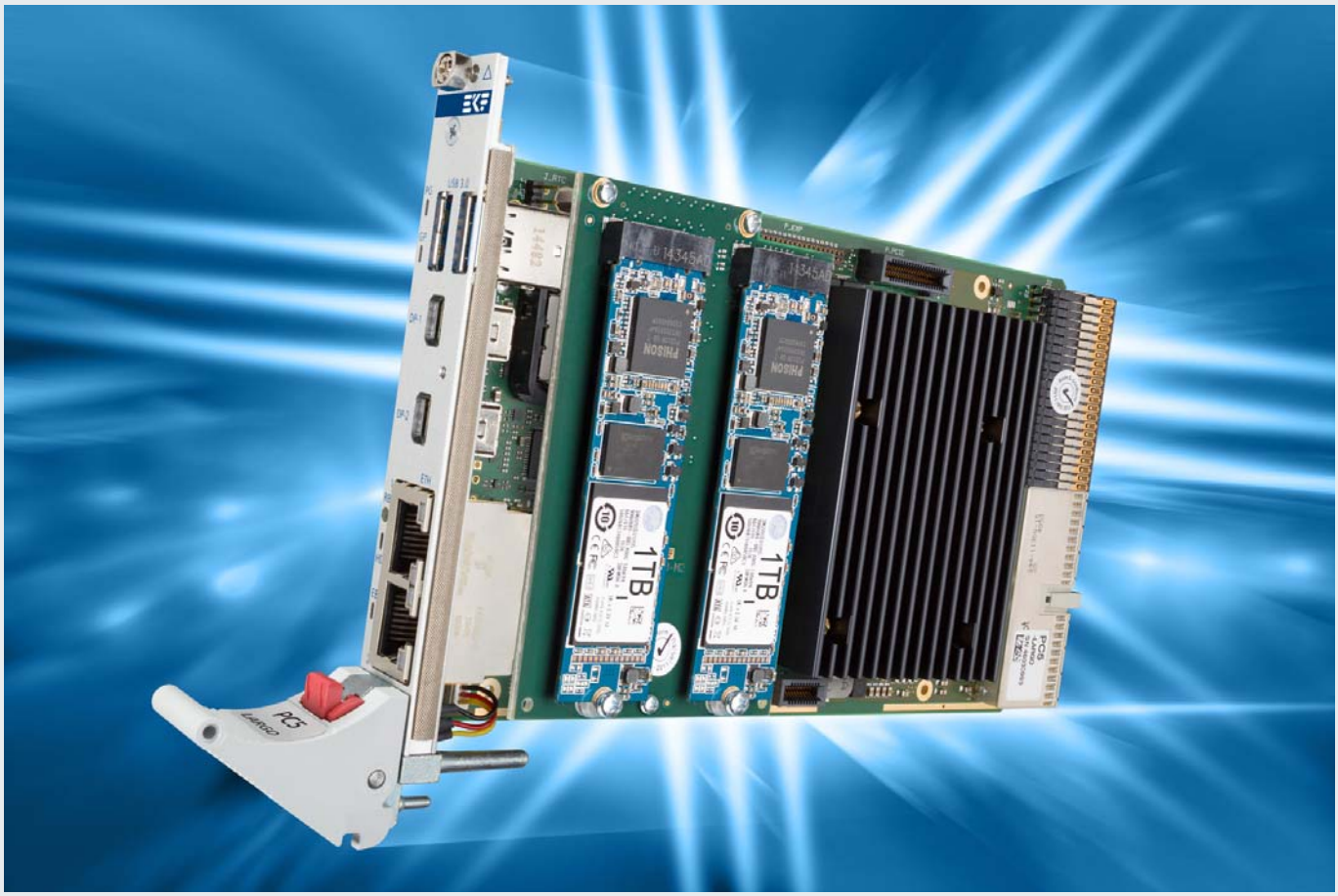


Contents

About this Manual

This manual describes the technical aspects of the PC5-LARGO, required for installation and system integration. It is intended for the experienced user only.

Edition History

Ed.	Contents/Changes	Author	Date
1	User Manual PC5-LARGO, english, preliminary edition Text #8556, File: pc5_ug.wpd	jj	20 June 2017
2	Fixed a mixup regarding external power reset signal via J2 C17	jj	11 August 2017
2.1	Added Intel® AMT support to table 'Feature Summary'	jj	6 November 2017
2.2	Warning regarding usage in a 64-bit classic environment also added to table 'Backplane Connector J2' (was already enclosed in section 'CompactPCI® PlusIO')	jj	7 December 2017
3.0	Removed PR1-RIO (obsolete)	jj	8 March 2018
4	Added Power requirements	gn	2018-08-03
5	Corrected typo in Status Register CMD_STAT1 Bit 4	gn	2020-07-03

Related Documents

Related Information	
PC5-LARGO Home	www.ekf.com/p/pc5/pc5.html
PC5-LARGO User Guide	www.ekf.com/p/pc5/pc5_ug.pdf

Related Documents CompactPCI® Serial & CompactPCI® PlusIO	
CompactPCI® Serial & PlusIO Overview	www.ekf.com/s/smart_solution.pdf
CompactPCI® PlusIO Home	www.ekf.com/p/plus.html
CompactPCI® Serial Home	www.ekf.com/s/serial.html

Related Documents Mezzanine Modules and Side Cards	
C40 ... C48 Series Mezzanine Storage Modules	www.ekf.com/c/ccpu/c4x_mezz_ovw.pdf
C48-M2 Dual M.2 SATA SSD Mezzanine Storage Module	www.ekf.com/c/ccpu/c48/c48.html
PCL-CAPELLA Mezzanine Side Card	www.ekf.com/p/pcl/pcl.html
PCS-BALLET Mezzanine Side Card	www.ekf.com/p/pcs/pcs.html
SCS-TRUMPET Mezzanine Side Card	www.ekf.com/s/scs/scs.html

Ordering Information
For popular PC5-LARGO SKUs please refer to www.ekf.com/liste/liste_21.html#PC5
For popular Mezzanine Side Cards please refer to www.ekf.com/liste/liste_20.html#C40

Nomenclature

Signal names used herein with an attached '#' designate active low lines.

Trade Marks

Some terms used herein are property of their respective owners, e.g.

- Core™ i7: ® Intel
- CompactPCI, CompactPCI PlusIO, CompactPCI Serial: ® PICMG
- Windows: ® Microsoft
- EKF, ekf system: ® EKF

EKF does not claim this list to be complete.

Legal Disclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

Standards

Reference Documents		
Term	**Document**	**Origin**
CFast™	CFast™ Specification Rev. 1.0	www.compactflash.org
CompactPCI®	CompactPCI Specification, PICMG® 2.0 R3.0, Oct. 1, 1999	www.picmg.org
CompactPCI® PlusIO	CompactPCI PlusIO Specification, PICMG® 2.30 R1.0, November 11, 2009	www.picmg.org
CompactPCI® Serial	CompactPCI Serial Specification, PICMG® CPCI-S.0 R1.0, March 2, 2011	www.picmg.org
DisplayPort	VESA DisplayPort Standard Version 1.2 December 22, 2009 VESA Mini DisplayPort Connector Standard Ver. 1 October 26, 2009	www.vesa.org
DVI	Digital Visual Interface Rev. 1.0 Digital Display Working Group	www.ddwg.org
Ethernet	IEEE Std 802.3, 2000 Edition	standards.ieee.org
Precision Time Protocol	IEEE Std 1588-2008, July 24, 2008	standards.ieee.org
LPC	Low Pin Count Interface Specification, Revision 1.1	developer.intel.com/design/chipsets/industry/lpc.htm
HD Audio	High Definition Audio Specification Rev.1.0	www.intel.com/design/chipsets/hdaudio.htm
PCI Express®	PCI Express® Base Specification 3.0	www.pcisig.com
SATA	Serial ATA 2.5/2.6 Specification Serial ATA 3.0 & 3.1 Specification	www.sata-io.org
TPM	Trusted Platform Module 2.0	www.trustedcomputinggroup.org
UEFI	Unified Extensible Firmware Interface UEFI Specification Version 2.5 ACPI Specification Version 6.0	www.uefi.org
USB	Universal Serial Bus 3.0 Specification, Revision 1.0 November 12, 2008	www.usb.org

Overview

The PC5-LARGO is a rich featured high performance 4HP/3U CompactPCI® PlusIO CPU board, equipped with a 5th generation Intel® Core™ mobile processor (Broadwell quad-core). The PC5-LARGO front panel is provided with two Gigabit Ethernet jacks, two USB 3.0 receptacles, and two mDP connectors (DisplayPort 1.2 MST, 4k UHD).

Local expansion mezzanine boards (side cards) are available for additional front panel and/or rear I/O, resulting in an 8HP front panel width assembly unit.

The PC5-LARGO can be equipped with up to 24GB DDR3L ECC RAM. Up to 8GB memory-down are provided for rugged applications, and another 16GB are available via the SO-DIMM socket. Low profile SSD mezzanine modules are available as on-board mass storage solution.

The PC5-LARGO backplane connectors comply with the PICMG® CompactPCI® PlusIO system slot specification, suitable for a rear I/O module or hybrid CompactPCI® Serial system via J2. Across J1, the PC5-LARGO is backwards compatible to classic CompactPCI® systems.

CompactPCI® PlusIO (PICMG 2.30) is a standard for rear I/O across J2, specified by the PICMG®. High speed signal lines (PCI Express®, SATA, Gigabit Ethernet and USB) are passed from the PC5-LARGO through the special UHM connector to the backplane, for usage either on a PlusIO rear I/O transition module, or CompactPCI® Serial card slots.

CompactPCI® Serial (PICMG CPCIS.0) defines a completely new card slot, based on PCI Express®, SATA, Gigabit Ethernet and USB serial data lines. On a hybrid backplane, both card styles can reside, CompactPCI® and CompactPCI® Serial, with the PC5-LARGO in the middle as system slot controller for both backplane segments.

The PC5-LARGO is equipped with a set of local expansion interface connectors, which can be optionally used to attach a mezzanine side board. A variety of expansion cards is available, e.g. providing legacy I/O and additional PCI Express® based I/O controllers such as SATA, USB 3.0 and Gigabit Ethernet, or a third video output. Most mezzanine side cards can accommodate in addition a 2.5-inch drive.

Typically, the PC5-LARGO and the related side card would come as a readily assembled 8HP unit. As an alternate, low profile Flash based mezzanine storage modules are available that fit on the PC5-LARGO while maintaining the 4HP profile. The C48-M2 module e.g. is equipped with two fast M.2 SATA Solid State Drives (SSD), which is suitable for installation of any popular operating system.

Technical Features

Feature Summary

Feature Summary

General

- CompactPCI® PlusIO (PICMG® CPCI 2.30) System Slot Controller
- Form factor single size Eurocard (board dimensions 100x160mm²)
- Mounting height 3U
- Front panel width 4HP (8HP/12HP assembly with optional mezzanine side card)
- Front panel I/O connectors for typical system configuration (2 x USB3, 2 x Mini DisplayPort, 2 x GbE)
- Backplane communication via CompactPCI® J1 and J2 hard metric connectors
- J1 Connector for PICMG® CompactPCI® 32-Bit support
- J2 Connector (UHM high speed) for CompactPCI® PlusIO support (4 x PCIe Gen2, 4 x SATA 3G/6G*, 4 x USB, 2 x GbE)
- J2 PlusIO configuration allows for either CompactPCI® Serial backplane usage or rear I/O module attachment
- On-board PCIe x 4 Gen2 mezzanine expansion option (side card)
- On-board SATA x 4 6G mezzanine expansion option for mass storage modules or side cards
- On-board DisplayPort (3rd video output) mezzanine expansion option for side cards
- Side cards and low profile mass storage modules available as COTS and also as custom specific

Processor

- 5th Generation Intel® Core™ CPU (Broadwell H)
- i7-5850EQ • 4 Cores • 2.7GHz (TB 3.4GHz) • 47/37W TDP/cTDP • GT3e-6200 Intel® Iris™ Pro graphics 1GHz • 6MB LLC • vPRO™/AMT
- i7-5700EQ • 4 Cores • 2.6GHz (TB 3.4GHz) • 47/37W TDP/cTDP • GT2-5600 Intel® HD graphics 1GHz • 6MB LLC • vPRO™/AMT

Firmware

- Phoenix® UEFI (Unified Extensible Firmware Interface) with CSM*
- Fully customizable by EKF
- Secure Boot and Measured Boot supported - meeting all demands as specified by Microsoft®
- Windows®, Linux and other (RT)OS' supported
- Intel® AMT supported (disabled by default, must be enabled via BIOS setup)

** CSM (Compatibility Support Module) emulates a legacy BIOS environment, which allows to boot a legacy operating system such as DOS, 32-bit Windows and some RTOS'*

Feature Summary

Main Memory

- Integrated memory controller up to 24GB DDR3L 1600 +ECC
- DDR3L +ECC soldered memory up to 8GB
- DDR3L +ECC SO-DIMM memory module socket up to 16GB

Graphics

- Integrated graphics engine, 3 symmetric independent displays
- 3D HW acceleration DX11.1, OpenCL 1.2, OpenGL 4.3, ES 2.0
- HW media acceleration DXVA 2, VAAPI
- HW video decode H264, SVC, AVC, MVC, MPEG-2, MJPEG, JPEG large frame support, VC-1, VP8
- HW video encode H264, SVC, AVC, MVC, MPEG-2
- Content protection PUMA, PAVP, HDCP
- Front panel options: Dual Mini-DisplayPort (mDP) or single VGA connector
- 3rd DisplayPort connector via mezzanine side card optional
- DisplayPort™ 1.2 Multi-Stream Transport (MST) - display daisy chaining
- Max Resolution 4096 x 2304 @60Hz (any DisplayPort), 1920 x 1200 (VGA)
- 4k x 2k @24Hz supported for Blu-ray playback
- Integrated audio

Networking

- Up to 4 networking interfaces in total - 2 x front RJ45 GbE, 2 x backplane GbE via J2
- 1000BASE-T, 100BASE-TX, 10BASE-T connections
- Front port 1 - I217LM with Intel® AMT support
- Front port 2 - Intel® I210-IT -40°C to +85°C operating temperature GbE NIC w. integrated PHY
- Front port option M12 X-coded connectors (replacement for RJ45, requires 8HP front panel width)
- IPv4/IPv6 checksum offload, 9.5KB Jumbo Frame support, EEE Energy Efficient Ethernet
- IEEE 802.1Qav Audio-Video-Bridging (AVB) enhancements for time-sensivitive streams
- IEEE 1588 and 802.1AS packets hardware-based time stamping for high-precision time synchronization
- Backplane Gigabit Ethernet w. 2 x I210-IT NIC

Chipset

- Intel® QM87 Lynx Point Platform Controller Hub (PCH)
- 8 x PCIe Gen2 5GT/s
- 6 x SATA 6G
- 10 x USB2, 4 x USB3
- LPC, Audio, Legacy

Feature Summary

On-Board Building Blocks

- Additional on-board controllers, PCIe® based
- 3 x Gigabit Ethernet controllers Intel® I210IT
- 1 x Gigabit Ethernet PHY Intel® I217LM
- PCIe® to PCI® Bridge PLX 8112
- PCIe® Gen2 packet switch PLX 8608
- SATA 3G/6G* RAID controller Marvell® 88SE9230, ARM powered subsystem for host CPU offload

** Marvell SATA RAID controller setup for 3Gbps by default*

Security

- Trusted Platform Module
- TPM 2.0 for highest level of certified platform protection
- Infineon Optiga™ SLB 9665 cryptographic processor
- Conforming to TCG 2.0 specification
- AES hardware acceleration support by 5th Gen processor series (Intel® AES-NI)

Front Panel I/O (4HP)

- 2 x Gigabit Ethernet RJ45 (1 = PCH & I217LM - Intel® AMT support, 2 = I210IT)
- 2 x DisplayPort (from processor integrated HD graphics engine, mDP style receptacles, optional cable connector retainer available)
- 2 x USB 3.0 Type-A

CompactPCI® & CompactPCI® PlusIO Backplane Resources

- PICMG® CompactPCI® 2.0 CPU card & system slot controller for J1 based 32-bit PCI® systems, 33/66MHz
- PICMG® CompactPCI® 2.30 J2 UHM connector according to CompactPCI® PlusIO
- J2 can be used to enable CompactPCI® Serial peripheral card slots for hybrid systems with a split backplane
- J2 can be used alternatively for a rear I/O module
- J2 is assigned to 4 x PCIe Gen2 5GT/s (from PCH), 4 x SATA 3G/6G* (from Marvell SATA hardware RAID controller), 4 x USB2 ports (from PCH), 2 x Gigabit Ethernet (I210IT networking controllers)

** Marvell SATA RAID controller setup for 3Gbps by default*

Feature Summary

Local Expansion and Mass Storage Solutions

- Mezzanine side card connectors for optional local expansion
- P-EXP - 2 x USB 2.0 & Legacy (from PCH)
- P-DP3 - 3rd DisplayPort video (from Intel® Core™ CPU)
- P-HSE - 4 x SATA 6G & 4 x USB 2.0 (from PCH)
- P-PCIE - PCIe Gen2 5GT/s 1 link x 4 lanes or 4 links x 1 lane (from on-board PCIe® switch)

- 4HP Low profile mezzanine module options (to be ordered separately)
- CFast™ Card with C41-CFAST mezzanine module
- SATA 1.8-Inch Solid State Drive with C42-SATA mezzanine module
- Dual mSATA SSD with C47-MSATA mezzanine module
- Dual M.2/NGFF SATA SSD 2230 - 2280 size with C48-M2 mezzanine module
- Custom specific module design

- 8HP/12HP Mezzanine side card options (to be ordered separately)
- PCL-CAPELLA - multi function side card
- PCS-BALLET - multi function side card
- SCS-TRUMPET - multi function side card
- C32-FIO - 2 x COM RS-232, USB, PS/2 (12HP assembly)
- Variety of other side cards available
- Custom specific side card design

Environmental & Regulatory

- Suitable e.g. for industrial, transportation & instrumentation applications
- Designed & manufactured in Germany - ISO 9000 quality management certified
- Long term availability
- Rugged solution
- Coating, sealing, underfilling on request
- Lifetime application support
- RoHS compliant
- Operating temperature 0°C to +70°C
- Operating temperature -40°C to +85°C (industrial temperature range) on request
- Storage temperature -40°C to +85°C, max. gradient 5°C/min
- Humidity 5% ... 95% RH non condensing
- Altitude -300m ... +3000m
- Shock 15g 0.33ms, 6g 6ms
- Vibration 1g 5-2000Hz
- MTBF 11.0 years (PC5-480D)
- EC Regulatory EN55022, EN55024, EN60950-1 (UL60950-1/IEC60950-1)

Feature Summary

RT OS Board Support Packages & Driver

- LynxOS - on request
- On Time RTOS-32 - on request
- OS-9 - on request
- QNX 4.x, 6.x - on request
- Real-Time Linux (RT Patch) - on request
- RTX - on request
- VxWorks 5.5 & 6.9 - on request
- VxWorks 7.0 - under development
- Others - on request

All items are subject to changes w/o further notice

Performance Rating

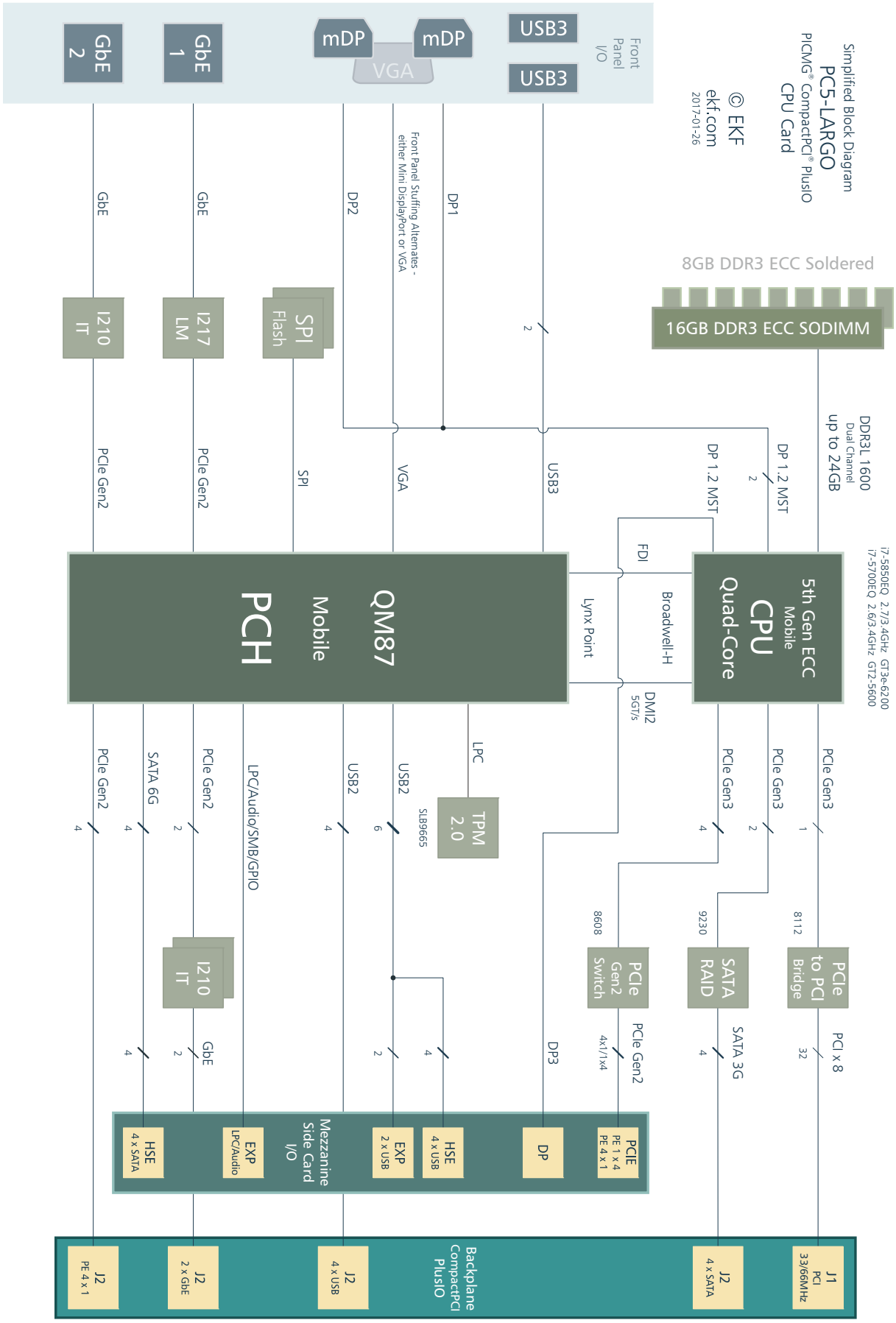
Performance Rating
tbd

Power Requirements

Power Requirements				
	Load Current [A] at +3.3V (+0.17V/-0.1V)		Load Current [A] at +5V (+0.25V/-0.15V)	
Board	Maximum Performance LFM / HFM / Turbo [1]	Windows 10 Idle LFM / HFM / Turbo [1]	Maximum Performance LFM / HFM / Turbo [1]	Windows 10 Idle LFM / HFM / Turbo [1]
PC5-830D	tbd / tbd / 2.5[2]	tbd / tbd / tbd[2]	tbd / tbd / 8.4	tbd / tbd / tbd
PC5-tbd	[2]	[2]		

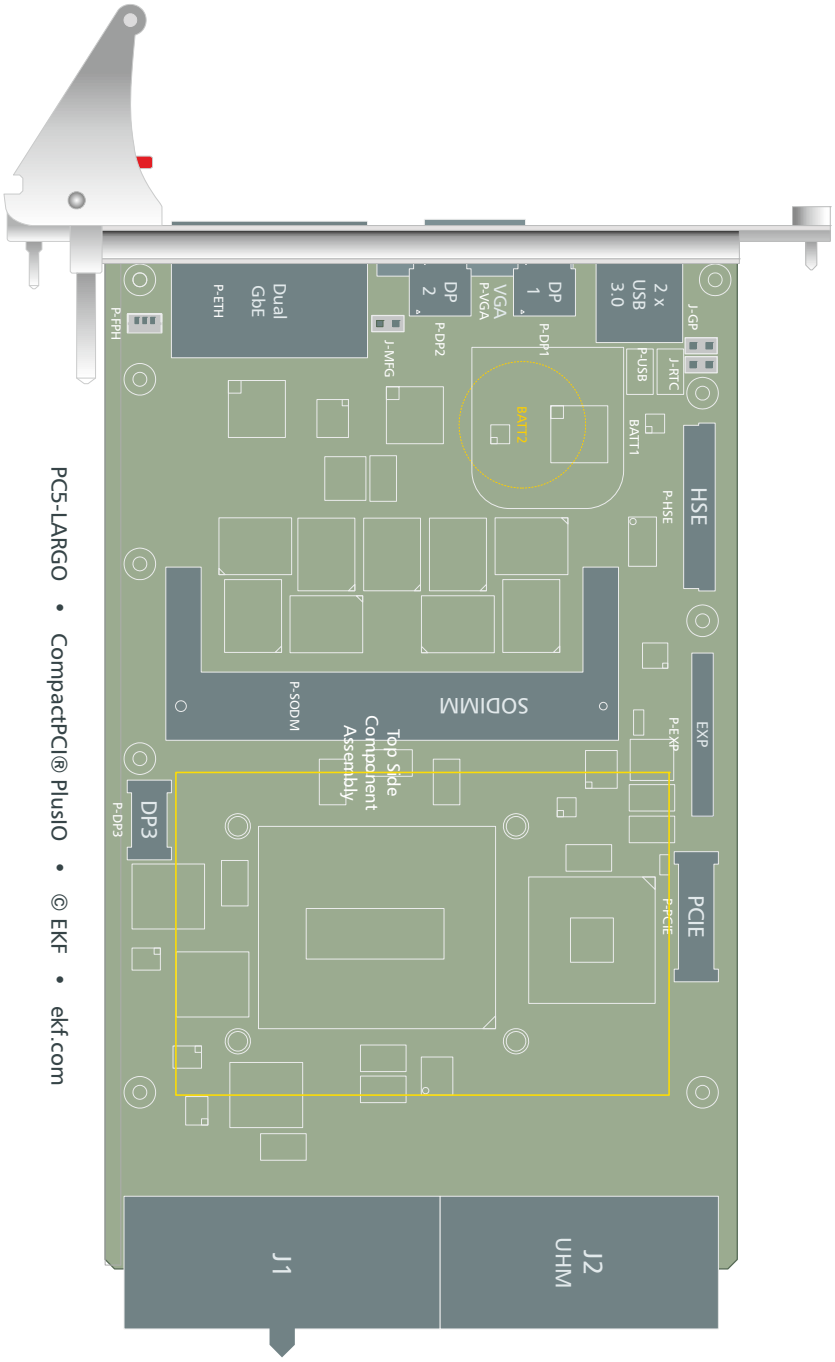
[1] Intel SpeedStep Frequence Modes LFM: Low Frequency Mode, HFM: High Frequency Mode.
[2] Add 200/600mA (link only/active) @1Gbps per Ethernet Port.

Block Diagram

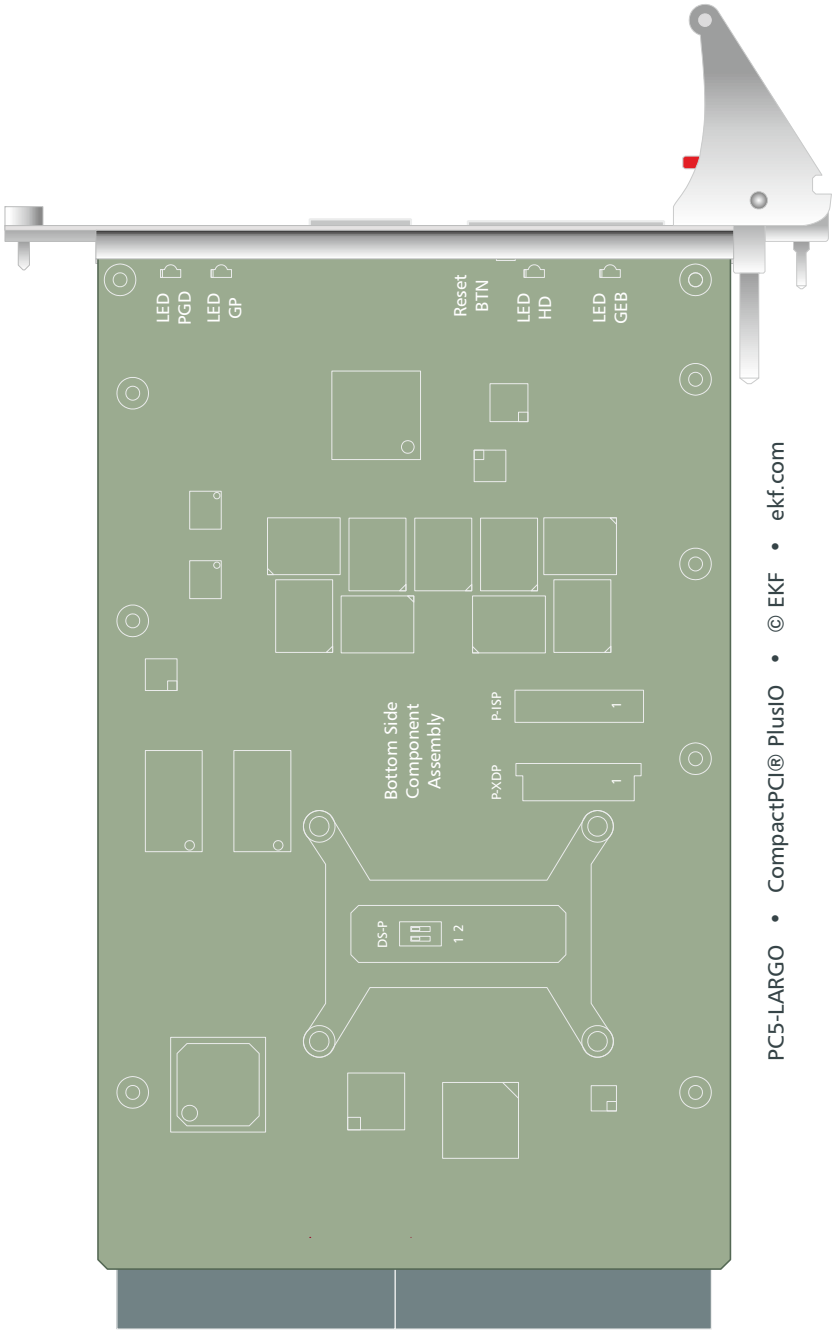


www.ekf.com/p/pc5/img/pc5_blk.pdf

Top View Component Assembly



Bottom View Component Assembly



Front Panel Connectors

ETH1/2	Dual Gigabit Ethernet RJ-45 receptacles with integrated indicator LEDs
DP1/2	Mini DisplayPort digital video output receptacle (VGA connector available as alternate)
USB1/2	Universal Serial Bus 3.0 type A receptacles
VGA	VGA analog video output connector (Mini DisplayPort connectors available as alternate)

Front Panel Switches & Indicators

EB	LED indicating Backplane Ethernet activity
FPH	Front Panel Handle with integrated switch (programmable function, power event button by default)
GP	General Purpose bicolour LED
HD	Bicoloured LED indicating any activity on SATA ports
PG	Power Good/Board Healthy bicolour LED
RB	System Reset Button (Option)

On-Board Connectors & Sockets

P-EXP	Utility EXPansion Interface Connector (LPC, USB, HD Audio, SMBus), interface to optional side board
P-HSE	High Speed Expansion Connector (4 x SATA, 4 x USB), interface to optional low profile mezzanine module or side board
P-PCIE	PCI Express® Expansion Interface Connector, interface to optional side board
P-DP3	Digital Display Interface Connector, interface to optional 3rd DisplayPort on side board
J1/J2	CompactPCI® Bus 32-bit (universal V(I/O)), 33MHz, PlusIO
P-SODM	204-pin DDR3L ECC Memory Module SDRAM PC5L-12800 Socket (ECC SODIMM)
P-XDP	CPU Debug Port [1)]

[1)] Connector populated on customers request only

Pin Headers

P-FPH	Pin header suitable for Front Panel Handle switch cable harness
P-ISP	PLD glue logic device programming connector, not populated

Jumpers

DS-P	Switches to configure link width and speed on P-PCIE
J-GP	Jumper to reset UEFI BIOS Setup to EKF Factory Defaults, IEEE 1588 Pulse per Second Output
J-MFG	Jumper to enter Manufacturing Mode, not populated
J-RTC	Jumper to reset RTC circuitry (part of PCH), not populated

Microprocessor

The PC5-LARGO is equipped with an Intel® Core™ i7 5th generation mobile ECC processor (code name "Broadwell"). This processor provides integrated graphics, memory controller and voltage regulators, which results in a very efficient platform design. As of current, Intel® offers two CPU versions suitable for the PC5-LARGO, differing mainly in the GPU integrated (the powerful GT3e-6200 Intel® Iris™ Pro graphics is provided with the i7-5850EQ only).

The processor is housed in a Micro FC-BGA package for direct soldering to the PCB, i.e. the chip cannot be removed or changed by the user.

The processors supported by the PC5-LARGO are running at core clock speeds up to 2.7GHz for quad core usage. Due to Enhanced Intel® SpeedStep® and Intel® Turbo Boost Technology each core can decrease or increase its nominal operating frequency. The clock speed is chosen depending on the power states of the processor cores/graphics engine, the currently required performance, and the actual core temperature.

Power is applied across the CompactPCI® connector J1 (3.3V, 5V). The processors core voltage is generated by a switched voltage regulator sourced from the 5V plane.

Intel® Core™ Processors Supported [1]									
Processor Number	Physical Cores	Core Clock nom./max. [GHz]	Cache [MB]	Gfx Clock [MHz]	Junction Temp. [°C]	TDP/ cTDP [W]	CPU ID	Stepping	SPEC Code
i7-5850EQ	4	2.7/3.4	6	GT3e 1000		47/ 37			
i7-5700EQ	4	2.6/3.4	6	GT2 1000		47/ 37			

[1] The processors listed are units with long life support.
[2] This processor may run with different TDPs configurable by BIOS settings.

Thermal Considerations

In order to avoid malfunctioning of the PC5-LARGO, take care of appropriate cooling of the processor and system, e.g. by a cooling fan suitable to the maximum power consumption of the CPU chip actually in use. The processor contains digital thermal sensors (DTS) that are readable via special CPU registers. DTS allows to get the temperatures of each CPU core separately.

Two further temperature sensors, located in the system hardware monitor LM87, allow for acquisition of the boards surface temperature and the thermal state of the onboard system memory channel. Beside this the LM87 also monitors most of the supply voltages. A suitable software on Microsoft Windows® systems to display both, the temperatures as well as the supply voltages, is 'Speedfan', which can be downloaded from the web. After installation, both temperatures and voltages can be observed permanently from the Windows® taskbar.

The PC5-LARGO is equipped with a passive heatsink. Its height takes into account the 4HP limitation in mounting space of a CompactPCI® board. In addition, a forced vertical airflow through the system enclosure (e.g. bottom mount fan unit) is strongly recommended (>20m^3/h or 2m/s (400LFM) around the CPU slot). Be sure to thoroughly discuss your actual cooling needs with EKF. Generally, the faster the CPU speed the higher its power consumption. For higher ambient temperatures, consider increasing the forced airflow to 3m/s (600LFM) or more.

The table showing the supported processors above give also the maximum power consumption (TDP) of a particular processor. Fortunately, the power consumption is by far lower when executing typical Windows® or Linux tasks. The heat dissipation increases when e.g. rendering software like the Acrobat Distiller is executed.

The Core™ processors support Intel's Enhanced SpeedStep® technology. This enables dynamic switching between multiple core voltages and frequencies depending on core temperature and currently required performance. The processors are able to reduce their core speed and core voltage in multiple steps down to 800MHz. Additional a reduction of the graphics core clock (down to 200MHz) and voltage is possible. This leads to an obvious reduction of power consumption resulting in less heating.

A further way to reduce power consumption is achieved by integrating the voltage regulators on the die of the 5th generation Core™ processors. This embedding allows the processor to regulate the voltages to each core, graphics, cache and other units separately depending on their performance needs. Parts that are currently idle may switched off to save power.

Main Memory

The PC5-LARGO features two channels of DDR3L SDRAMs with support of ECC (Error Correction Code). One channel is realized with 18 memory devices soldered to the board (Memory Down) and delivers a capacity of up to 8GB with a clock frequency of 1600MHz (PC5L-12800).

The 2nd channel provides a socket for installing a 204-pin ECC SODIMM module thus allowing a simple expansion of system memory (max. module height = 1.25 inch). Supported are unbuffered DDR3L ECC SODIMMs (72-bit) with V_{DD}=1.35V featuring on-die termination (ODT), according the PC5L-12800 specification. Minimum module size is 512MB; maximum module size is 16GB. Please note, that neither standard DDR3 SODIMMs nor DDR3L without ECC feature will work on PC5-LARGO.

It is recommended to add a SODIMM module with same size as the Memory Down to get best performance. Since some of the system memory is dedicated to the graphics controller a typically development of 2x8GB of memory is recommended to run operating systems like Windows®.

The memory controller supports symmetric and asymmetric memory organization. The maximum memory performance can be obtained by using the symmetric mode. When in this mode, the memory controller accesses the memory channels in an interleaved way. Since Core™ processors support Intels Flex Memory Technology, interleaved operation is not limited to systems using memory channels of equal capacity. In the case of unequal memory population the smaller memory channel dictates the address space of the interleaved accessible memory region. The remainder of the memory is then accessed in non-interleaved mode.

In asymmetric mode the memory always will be accessed in a non-interleaved manner with the drawback of less bandwidth. The only meaningful application of asymmetric mode is the special case when only one memory channel is populated (i.e. the SODIMM socket may be left empty).

The contents of the SPD EEPROM on the SODIMM is used by the BIOS at POST (Power-on Self Test) to get any necessary timing parameters to program the memory controller within the chipset.

Graphics Subsystem

The structure of the graphics subsystem has changed compared to the predecessor of the Intel 4th and 5th generation Core™ processor. The main graphics interfaces are based on the DisplayPort standard and are part of the processor. Only a few sideband signals (DDC/Auxiliary channel, hot plug detection) as well as the VGA interface is remained at the PCH QM87.

The PC5-LARGO offers two Mini DisplayPort (mDP) interfaces in the front panel. Adapters to convert Mini DisplayPort to any other popular interface standard are available.

A 3rd DisplayPort is fed to the on-board connector P-DP3. EKF expansion boards like the PCS-BALLET provide the 3rd DisplayPort connector (standard type) via the common 8HP front panel.

As an alternate, the PC5-LARGO can be equipped with an ordinary HD D-Sub 15-lead connector (VGA style). This connector is suitable for analog signals only. Nevertheless also flat-panel displays can be attached to the D-Sub connector but with minor reduced image quality.

Independent from the video connector actually in use, Mini DisplayPort or VGA, the VESA DDC standard is supported. This allows to read out important parameters, e.g. the maximum allowable resolution, from the attached monitor. DDC power, +3.3V on DisplayPort connectors, is delivered via electronic switches to protect the board from an external short-circuit condition (1.5A) and to prevent back current flows. On the VGA interface a resettable fuse (0.5A) is used supply the +5V DDC power.

Graphics drivers for the Intel® GPU are an inherent part of popular operating systems, or can be downloaded from the Intel® website.

LAN Subsystem

The Ethernet LAN subsystem is composed of four Gigabit Ethernet ports: One Intel i217LM Physical Layer Transceiver (PHY) using the PCH QM87 internal MAC and three Intel i210IT Gigabit Ethernet Controllers. These devices provide also legacy 10Base-T and 100Base-TX connectivity. Two of the Ethernet ports are fed to two RJ45 jacks located in the front panel, the others are attached to the CompactPCI® Serial interface on J2. Each port includes the following features:

- One PCI Express lane per Ethernet port (250MB/s)
- 1000Base-Tx (Gigabit Ethernet), 100Base-TX (Fast Ethernet) and 10Base-T (Classic Ethernet) capability.
- Half- or full-duplex operation.
- IEEE 802.3u, 802.3ab Auto-Negotiation for the fastest available connection.
- Jumperless configuration (complete software-configurable).

Two bicoloured LEDs integrated into the dedicated RJ-45 connector in the front panel are used to signal the LAN link, the LAN connection speed and activity status. A further bicoloured LED in front panel labelled EB displays the state of the backplane network ports.

Each device is connected by a single PCI Express lane to the PCH. Their MAC addresses (unique hardware number) are stored in dedicated FLASH/EEPROM components. The Intel Ethernet software and drivers for the i217LM and i210IT are available from Intel's World Wide Web site for download.

When managing the board by Intel Active Management Technology (iAMT), the dedicated network port to do so is accessible by the RJ45 connector GbE1 (the upper port within the front panel).

Although any of the i210 controllers support the IEEE 1588 Precision Time Protocol, the one connected to GbE2 (the lower port within the front panel) is capable to generate Pulse per Second (PPS) and Pulse per Minute (PPM) signals that may be routed to the jumper J-GP and the CompactPCI® Serial connector P1. These signals can be used to trigger events on Mezzanine Side Boards or Peripheral Boards. The following routing is possible by UEFI BIOS settings:

- Pulse per Second (PPS): J-GP Pin 1 and CompactPCI® Pin J3 (signal SATA-SCL)
- Pulse per Minute (PPM): CompactPCI® Pin H3 (signal SATA-SDO)

Serial ATA Interface (SATA)

The PC5-LARGO provides a total of eigth serial ATA (SATA) ports, derived from two independent SATA controllers. A SATA controller is located within the QM87 Platform Controller Hub that holds 4 SATA interfaces and in a separate SATA host controller Marvell 88SE9230, providing four SATA ports, all 6Gbps capable.

The QM87 ports are fed to the high speed expansion connector P-HSE. This connector allows the installation of low profile expansion boards like C41-CFAST or C42-SATA to attach the popular CFast cards or Micro SATA SSDs (1.8-inch) respectively. Another mezzanine is the C47-MSATA, a carrier for two MSATA SSD modules.

The Marvell 88SE9230 is an SATA 6Gbps AHCI/RAID I/O controller connected via two PCI Express lanes (1GB/s) to the QM87. It supports hardware RAID levels 0, 1 and 10. All of its SATA ports are used to supply the CompactPCI® PlusIO SATA interfaces on the backplane or rear I/O module via the J2 UHM connector. *Please note, that the CompactPCI® PlusIO specification refers to SATA data rates of 1.5Gbps and 3Gbps. EKF has tested successfully also 6G over the backplane with sample devices, but cannot guarantee this data rate under any condition. Other devices and other backplane brands/types in use may cause a different result. Hence, for optimum reliability, the Marvell SATA controller will be initialized for 3Gbps on all ports by default. The J2 backplane SATA 6Gbps configuration would be available however as a PC5-LARGO option on special request (altered content for the Marvell 88SE9230 attached SPI Flash). EKF recommends that customers validate their particular SATA 6G application thoroughly, since SATA channel data errors can decrease the performance considerably.*

A LED named HD located in the front panel, signals disk activity status of any QM87 SATA devices (green) or 88SE9230 devices (yellow).

Additionally a variety of side cards is available, suitable for mounting on the PC5-LARGO in a 4HP (20.32mm) distance (resulting in 8HP front panel width for the assembly). Some of these side boards can accommodate a SATA drive, e.g. a 2.5-inch SSD.

Available for download from Intel's web site are drivers for popular operating systems, e.g. Windows® and Linux.

Drivers and software to manage the RAID configuration of the 88SE9230 (Windows® application) is provided by Marvell and can be downloaded from EKF's website.

PCI Express® Interface

The PC5-LARGO is provided with several PCI Express (PCIe) lanes for I/O expansion. Four PCI Express Gen 2 lanes (5GT/s), originating from the QM87, are available at the backplane connector J2. Another four PCI Express lanes are provided by the Intel Core™ i7 processor to the J-PCIE connector. A small DIP switch (DS-P) located on the backside of the board are used to configure different lane widths to each of both downstream interfaces and to choose the interface transfer rate. Possible settings are

- Single link x 4 lanes to J-PCIE
- Four links x 1 lane to J-PCIE
- 2.5GT/s or 5GT/s transfer speed

See section “Configuration PCI Express Switch (DS-P)” for details.

Universal Serial Bus (USB)

The PC5-LARGO is provided with twelve USB ports. All of them are USB 2.0 capable, but two ports, routed to front panel connectors, are also supporting the USB 3.0 SuperSpeed standard.

The USB 2.0 interfaces are distributed to the front panel (two ports), two to the expansion board interface connectors J-EXP, four to the high speed expansion connector J-HSE, and four ports are available across the backplane connector J2.

The front panel USB connectors can source a minimum of 1.5A/5V each, over-current protected by two electronic switches. Protection for the USB ports on the expansion interfaces and on the J2 PlusIO connector is located on expansion boards. The USB xHCI and two EHCI controllers handling the USB port operation at SuperSpeed, high-speed, full-speed and low-speed are integrated into the QM87 PCH.

Utility Interfaces

Besides the high speed mezzanine interface connectors P-HSE and P-PCIE, the PC5-LARGO is provided with the utility interface expansion connector socket P-EXP. This connector comprises several interfaces, which may be useful for system expansion on mezzanine cards, as an option:

- HD Audio
- LPC (Low Pin Count)
- SMBus
- 2 x USB

The SMBus is controlled by the QM87 platform controller hub. The SMBus signal lines on the P-EXP utility expansion connector can be switched on/off under software control (PCH GPIO) in order to isolate external components in case of an I^2C address conflict.

The HD Audio port requires an additional audio codec, as provided e.g. on the PCS-BALLET side card.

The LPC bus presents an easy way to add legacy interfaces to the system. EKF offers a variety of mezzanine expansion boards (side cards), to be attached on top of the PC5-LARGO, featuring all classic Super-I/O functionality, for example the PCS-BALLET. Access to the connectors PS/2 (mouse, keyboard), COM, USB and audio in/out is given directly from the front panel.

Real-Time Clock

The PC5-LARGO has a time-of-day clock and 100-year calendar, integrated into the QM87 PCH. A battery on the board keeps the clock current when the computer is turned off. The PC5-LARGO uses a holder to keep a BR2032 lithium coin cell, giving an autonomy of more than 5 years. Under normal conditions, replacement should be superfluous during lifetime of the board.

Alternately a BR2032 battery can be soldered in the board when board coating or shock/vibration is an interest.

In applications were the use of a battery is not permitted, a SuperCap can be soldered instead of the battery.

SPI Flash

The UEFI and iAMT firmware is stored in flash devices with Serial Peripheral Interface (SPI). Up to 16MByte of code, firmware and user data may be stored nonvolatile in these SPI Flashes.

The SPI Flash contents can be updated by a DOS or Linux based tool. This program and the latest PC5-LARGO UEFI binary are available from the EKF website. Read carefully the enclosed instructions. If the programming procedure fails e.g. caused by a power interruption, the PC5-LARGO may no more be operable. In this case you would possibly have to send in the board, because the Flash device is directly soldered to the PCB and cannot be changed by the user.

Reset

The PC5-LARGO is provided with several supervisor circuits to monitor supply rails like the CPU core voltage, 1.5V, 3.3V or 5V.

To force a manual board reset, the PC5-LARGO offers a small tactile switch within the front panel. This push-button is indent mounted and requires a tool, e.g. a pen to be pressed, preventing from being inadvertently activated.

The handle within the front panel contains a micro switch that is used to generate a power button event. By pressing the handle's red push button a pulse is triggered.
Animated GIF: www.ekf.com/c/ccpu/img/reset_400.gif

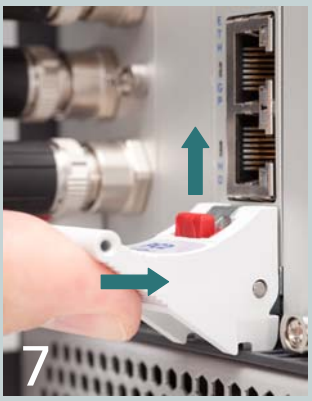
NOTE: To prevent the board to cause a power button override, the handle should be closed immediately after unlocking the front panel handle. A power button override is triggered by opening the front panel handle for at least 4 seconds, which results in bringing the board to power state S5. In case of entering this state, unlock and lock the front panel handle a 2nd time to reenter normal power state S0 again. See also section 'PG (Power Good) LED' to see how the PC5-LARGO indicates the different power states.

WARNING: The PC5-LARGO will enter the power state S5 if the front panel handle is not closed properly when the system powers up. An open handle is signalled by a yellow blinking 'PG LED'.

The manual reset push-button and the power button functionality of the front panel handle could be passivated by BIOS settings.

An alternative (and recommended) way to generate a system reset is to activate the signal PRST# located on CompactPCI® PlusIO connector J2 pin C17. Pulling this signal to GND will have the same effect as to push the tactile reset switch.

The healthy state of the PC5-LARGO is indicated by the LED PG (Power Good) located in the front panel. This bicoloured LED signals different states of the board (see section below). As soon as this LED begins to lite green, all power voltages are within their specifications and the reset signal has been deasserted.



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Watchdog

An important reliability feature is a software programmable watchdog function. The PC5-LARGO contains two of these watchdogs. One is part of the QM87 PCH and also known as TCO Watchdog. A detailed description is given in the QM87 data sheet. Operating systems like Linux offer a driver interface to the TCO watchdog.

The behaviour of the 2nd watchdog is defined within a PLD of the PC5-LARGO, which activates/deactivates the watchdog and controls its time-out period. The time-out delay is adjustable in the steps 2, 10, 50 and 255 seconds. After alerting the WD and programming the time-out value, the related software (e.g. application program) must trigger the watchdog periodically. For details on programming the watchdog see section “Board Control and Status Register (BCSR)”.

This watchdog is in a passive state after a system reset. There is no need to trigger it at boot time. The watchdog is activated on the first trigger request. If the duration between two trigger requests exceeds the programmed period, the watchdog times out and a full system reset will be generated. The watchdog remains in the active state until the next system reset. There is no way to disable it once it has been put on alert, whereas it is possible to reprogram its time-out value at any time.

Front Panel LEDs

The PC5-LARGO is equipped with four LEDs which can be observed from the front panel. Three of these LEDs are labelled according to their primary meaning, but should be interpreted altogether for system diagnosis:

LED			Status
PG Green/Red	GP Green/Red	HD Green/Yellow	
OFF	GREEN	GREEN	Sleep State S5 (Soft Off)
OFF	GREEN	OFF	Sleep State S4 (Suspend to Disk/Hibernate)
OFF	OFF	GREEN	Sleep State S3 (Suspend to RAM/Standby)
GREEN	RED BLINK	X	After Reset
GREEN	X	X	Board Healthy and in S0 State
YELLOW BLINK	X	X	Front panel handle is unlocked
RED	X	X	Hardware Failure - Power Fault
RED BLINK	X	X	Software Failure

PG (Power Good) LED

The PC5-LARGO offers a bicolour LED labelled PG located within the front panel. After system reset, this LED defaults to signal different power states:

- Off Sleep state S3, S4 or S5
- Green Healthy
- Yellow blink Front panel handle open
- Red steady Hardware failure
- Red blink Software failure

To enter the PG LED state *Software Failure,* the bit PGLED in the board control register CTRLL_REG must be set. The PG LED remains in this red blinking state until this bit is cleared. After that it falls back to its default function.

GP (General Purpose) LED

This programmable bicolour LED can be observed from the PC5-LARGO front panel. The status of the red part within the LED is controlled by the GPIO18 of the PCH QM87. Setting GPIO18 to “1" will switch on the red LED. Turning on or off the green LED is done by setting the bit GPLED in the board control register CTRLH_REG.

The GP LED is not dedicated to any particular hardware or firmware function with exception of special power states of the LED PG as described above. Nevertheless, a red blinking GP LED is an indication that the BIOS code couldn't start.

While the CPU card is controlled by the BIOS firmware, the GP LED is used to signal board status information during POST (Power On Self Test). After successful operating system boot, the GP LED may be freely used by customer software. For details please refer to www.ekf.com/p/pc5/firmware/biosinfo.txt.

HD (Hard Disk Activity) LED

The PC5-LARGO offers a bicoloured LED marked as HD placed within the front panel. This LED, when blinking green, signals activity on any device attached to the SATA ports of the QM87.

The yellow part of the HD LED shows activity on any of the 88SE9230 SATA ports.

As previously described, the green part of this LED may change its function dependent on the state of the LED PG.

EB (Ethernet Backplane) LED

To monitor the link status and activity on both Ethernet ports attached to the backplane via the CompactPCI® PlusIO connector J2 a single bicoloured LED is provided in the front panel. The states are decoded as follows:

1_ETH	2_ETH	LED EB
no link	no link	OFF
link	no link	GREEN
no link	link	YELLOW
link	link	GREEN/YELLOW

Blinking of the LED EB in the appropriate colour means that there is activity on the port.

Hot Swap Detection

The CompactPCI® specification added the signal ENUM# to the PCI bus to allow board hot swapping. This signal is routed to a GPIO (GPIO3 QM87 PCH) . An interrupt can be requested, if ENUM# changes, caused by insertion or removal of a peripheral board.

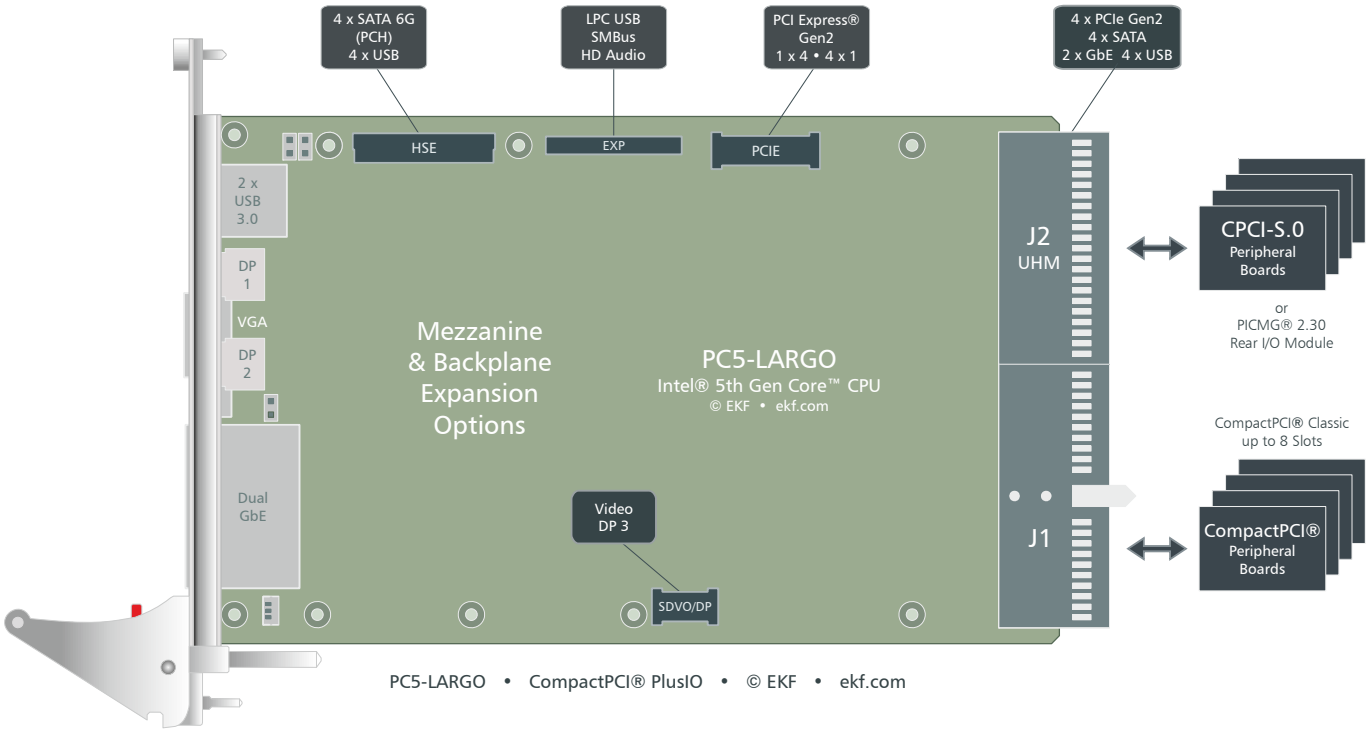
Note that the PC5-LARGO itself is not a hot swap device, because it makes no sense to remove the system controller from a CompactPCI® system. However, it is capable to recognize the hot swap of peripheral boards and to start software that is performing any necessary system reconfiguration.

Power Supply Status (PWR_FAIL#)

Power supply failures may be detected before the system crashes down by monitoring the signals DEG# or FAL#. These active low lines are additions to the CompactPCI® specification and may be driven by the power supply. DEG# signals the degrading of the supply voltages, FAL# there possible failure. On the PC5-LARGO DEG# is tied to VCC and FAL# is routed to QM87 PCH GPIO4.

Mezzanine Side Board Options

The PC5-LARGO is provided with several stacking connectors for attachment of a mezzanine expansion module (aka side board), suitable for a variety of readily available mezzanine cards (please refer to www.ekf.com/c/ccpu/mezz_ovw.pdf for a more comprehensive overview). EKF furthermore offers custom specific development of side boads (please contact sales@ekf.de).



PC5-LARGO • System Expansion Options

Most mezzanine expansion modules require an assembly height of 8HP in total, together with the CPU carrier board (resulting from two cards at 4HP pitch each). In addition, cropped low profile mass storage mezzanine modules can be attached to J-HSE, which maintain the 4HP envelope, for extremely compact systems. Furthermore these small size modules may be combined with some of the full-size expansion boards (that means an assembly comprised of three PCBs in total).

Sample Low Profile Mezzanine Module 4HP Assembly

Sample Mezzanine Side Card 8HP Assembly

P-EXP	
I/F Type	Controller
LPC (Low Pin Count)	PCH
HD Audio	PCH
SMBus	PCH (buffered)
2 x USB 2.0	PCH

P-HSE	
I/F Type	Controller
SATA1, SATA2, SATA3, SATA4	PCH
4 x USB 2.0	PCH

P-PCIE	
I/F Type	Controller
PCI Express® Gen2 1x4 or 4x1	PE Switch

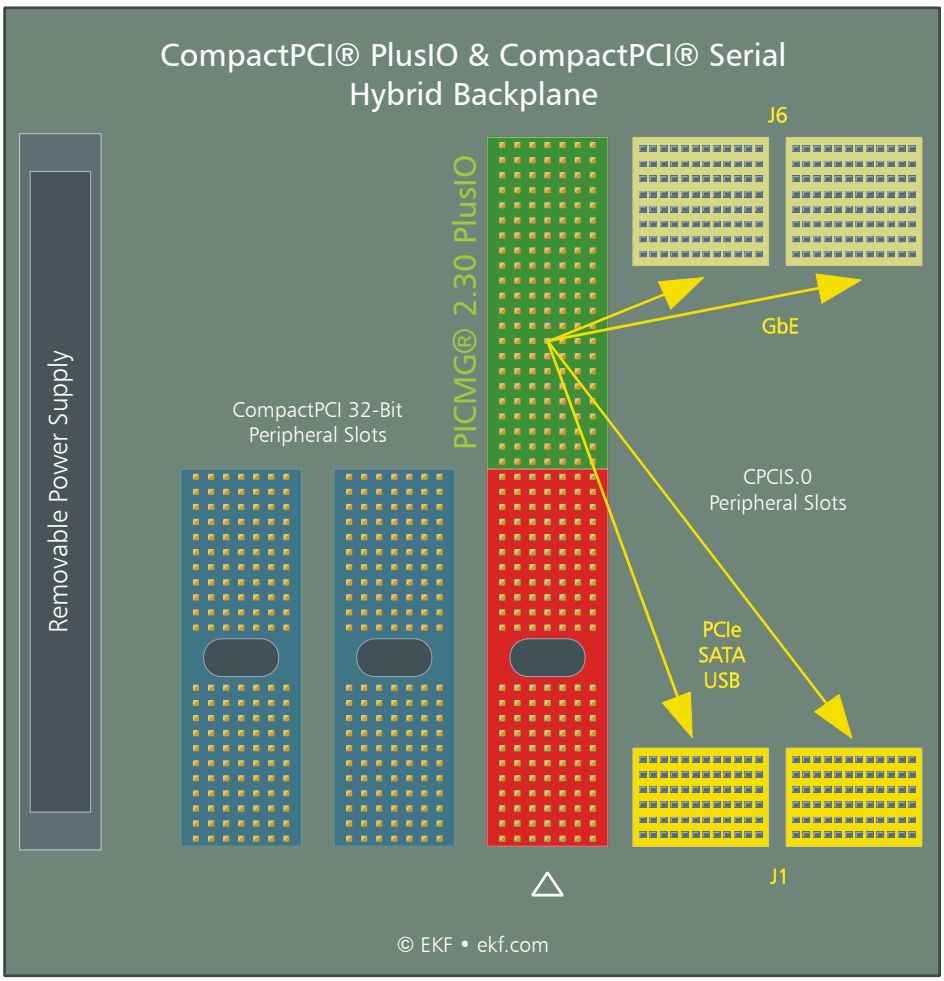
PC5-LARGO w. SCS-TRUMPET 8HP Assembly

CompactPCI® PlusIO

CompactPCI® PlusIO (PICMG® 2.30) is a standard for rear I/O across J2. High speed signal lines (PCI Express®, SATA, Gigabit Ethernet and USB) are passed from the PC5-LARGO through the special UHM J2 connector to the backplane, for usage either with a PlusIO rear I/O transition module, or CompactPCI® Serial card slots.

CompactPCI® Serial (PICMG® CPCIS.0) defines a completely new card slot, based on PCI Express®, SATA, Gigabit Ethernet and USB serial data lines. On a hybrid backplane, both card styles can reside, CompactPCI® and CompactPCI® Serial, with the PC5-LARGO in the middle as controller for both backplane segments.

The PC5-LARGO can be used in any system with a CompactPCI® PlusIO backplane according to the PICMG® 2.30 specification. Hybrid backplanes allow the configuration of systems with CompactPCI® Serial slots in addition to classic CompactPCI® boards.



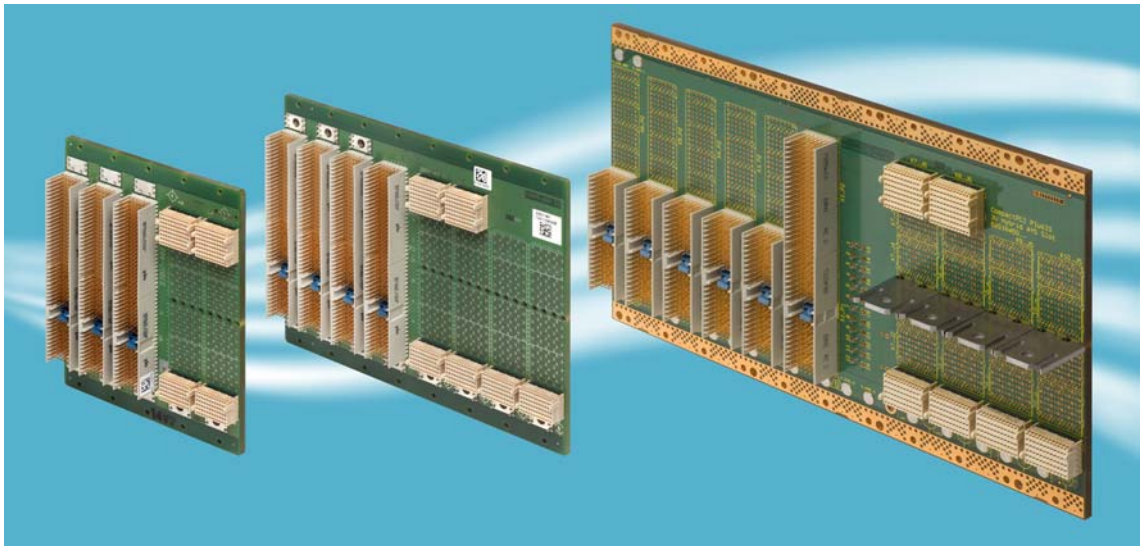
Sample Small Systems Hybrid Backplane

As an alternate to a hybrid backplane, the PC5-LARGO can be combined with a CompactPCI® PlusIO rear I/O transition module.

Warning:

Do not operate the standard PC5-LARGO in systems with a 64-bit CompactPCI® backplane. The J2/P2 pin assignment of a 64-bit CPCI backplane differs substantially from a CompactPCI® PlusIO backplane, which will result in a short circuit situation on several pins, causing permanent damage to the PC5-LARGO. For use together with a 64-bit CompactPCI® classic backplane, special PC5-LARGO versions are available on customer request, however supporting only 32-bit peripheral cards. The use of 64-bit CompactPCI® classic peripheral boards may cause problems.

CompactPCI® PlusIO CPU Card as System Controller in a Hybrid System



Sample Hybrid CompactPCI® & CompactPCI® Serial Backplanes

CompactPCI® PlusIO Rack

Small CompactPCI® PlusIO Box

Installing and Replacing Components

Before You Begin

Warnings

The procedures in this chapter assume familiarity with the general terminology associated with industrial electronics and with safety practices and regulatory compliance required for using and modifying electronic equipment. Disconnect the system from its power source and from any telecommunication links, networks or modems before performing any of the procedures described in this chapter. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage. Some parts of the system can continue to operate even though the power switch is in its off state.

Caution

Electrostatic discharge (ESD) can damage components. Perform the procedures described in this chapter only at an ESD workstation. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis or board front panel. Store the board only in its original ESD protected packaging. Retain the original packaging (antistatic bag and antistatic box) in case of returning the board to EKF for repair.

Installing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system

- Remove the board packaging, be sure to touch the board only at the front panel
- Identify the related CompactPCI® slot (peripheral slot for I/O boards, system slot for CPU boards, with the system slot typically most right or most left to the backplane)
- Insert card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- A card with onboard connectors requires attachment of associated cabling now
- Lock the ejector lever, fix screws at the front panel (top/bottom)
- Retain original packaging in case of return

Removing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system
- Identify the board, be sure to touch the board only at the front panel
- Unfasten both front panel screws (top/bottom), unlock the ejector lever
- Remove any onboard cabling assembly
- Activate the ejector lever
- Remove the card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- Store board in the original packaging, do not touch any components, hold the board at the front panel only

Warning

Do not expose the card to fire. Battery cells and other components could explode and cause personal injury.

EMC Recommendations

CE

In order to comply with the CE regulations for EMC, it is mandatory to observe the following rules:

- The chassis or rack including other boards in use must comply entirely with CE
- Close all board slots not in use with a blind front panel
- Front panels must be fastened by built-in screws
- Cover any unused front panel mounted connector with a shielding cap
- External communications cable assemblies must be shielded (shield connected only at one end of the cable)
- Use ferrite beads for cabling wherever appropriate
- Some connectors may require additional isolating parts

Recommended Accessories

Blind CPCI Front Panels	EKF Elektronik	Widths currently available (1HP=5.08mm): with handle 4HP/8HP without handle 2HP/4HP/8HP/10HP/12HP
Ferrit Bead Filters	Ask EKF	
Metal Shielding Caps	Ask EKF	

Replacement of the Battery

When your system is turned off, a battery maintains the voltage to run the time-of-day clock and to keep the values in the CMOS RAM. The battery should last during the lifetime of the PC5-LARGO.

However, some versions of PC5-LARGO are delivered with a battery holder which makes it possible for the user to replace the coin cell. Use a BR2032 cell as replacement part to ensure an extended temperature range. Be careful when removing the old cell and inserting the new one.

For boards with a soldered battery the old battery must be desoldered, and the new one soldered. We suggest that you send back the board to EKF for battery replacement.

Warning

Danger of explosion if the battery is incorrectly replaced or shorted. Replace only with the same or equivalent type. Do not expose a battery to fire.

Technical Reference

Local PCI Devices

The following table shows the on-board PCI devices and their location within the PCI configuration space. Several devices are part of the processor and platform controller hub QM87.

Bus #	Device #	Function #	Vendor ID	Device ID	Description
0	0	0	0x8086	0x0C04	Processor Host Bridge/DRAM Controller
0	1	0	0x8086	0x0C01	Processor PCI Express Controller
0	1	1	0x8086	0x0C05	Processor PCI Express Controller
0	2	0	0x8086	0x0416	Processor Integrated Graphics Device
0	3	0	0x8086	0x0C0C	Audio Controller
0	20	0	0x8086	0x8C31	USB xHCI Controller
0	22	0	0x8086	0x8C3A	Intel ME Interface #1
0	22	1	0x8086	0x8C3B	Intel ME Interface #2
0	22	2	0x8086	0x8C3C	Intel ME IDE Redirection
0	22	3	0x8086	0x8C3D	Intel ME Keyboard Text Redirection
0	25	0	0x8086	0x153A	PCH Gigabit LAN NC1 (i217LM)
0	26	0	0x8086	0x8C2D	USB EHCI Controller #2
0	27	0	0x8086	0x8C20	Intel High Definition Audio Controller
0	28	0	0x8086	0x8C10	PCH PCI Express Port 1
0	28	3	0x8086	0x8C16	PCH PCI Express Port 4
0	28	4	0x8086	0x8C18	PCH PCI Express Port 5
0	29	0	0x8086	0x8C26	USB EHCI Controller #1
0	31	0	0x8086	0x8C4F	LPC Bridge
0	31	2	0x8086	0x8C01 0x8C03 0x1E07	SATA: Non-AHCI/Non-RAID (Ports 0-3) [1] SATA: AHCI Mode [1] SATA: RAID Capable [2]
0	31	3	0x8086	0x8C22	SMBus Controller
0	31	5	0x8086	0x8C09	SATA: Non-AHCI/Non-RAID (Ports 4/5)
0	31	6	0x8086	0x8C24	Thermal Controller
1 [3]	00	0	0x1B4B	0x9230	SATA Host Controller (88SE9230)
2 [3]	00	0	0x8086	0x157B	Ethernet Controller NC2 (i210IT)
3 [3]	00	0	0x10B5	0x8618	PCIe Switch Root Port (PEX8618)
4 [3]	01,02,04 ...	0	0x10B5	0x8618	PCIe Switch Downstream Ports (PEX8618)
5 [3]	00	0	0x8086	0x157B	Ethernet Controller NC3 (i210IT)
6 [3]	00	0	0x8086	0x157B	Ethernet Controller NC4 (i210IT)

1) Depends on BIOS settings.

2) Depending on BIOS settings different RAID modes may lead to other Device IDs.

3) Bus number can vary depending on the PCI enumeration schema implemented in BIOS.

Local SMB Devices

The PC5-LARGO contains devices that are attached to the System Management Bus (SMBus). These are the SPD EEPROMs for the on-board memory or the possibly plugged SODIMM, a general purpose serial EEPROM, a supply voltage/temperature controlling device and a set of board control and status registers. Additional devices may be connected to the SMBus via the CompactPCI® Serial backplane signals I^2C_SCL (P1 B2) and I^2C_SDA (P1 B3), or pins 29/30 of the mezzanine expansion connector P-EXP.

Address	Description
0x58	Hardware Monitor/Memory Down Temperature Sensor (LM87)
0x5C	Board Control/Status
0xA0	SPD of On-board Memory
0xA4	SPD of SODIMM
0xAE	General Purpose EEPROM

Hardware Monitor LM87

Attached to the SMBus, the PC5-LARGO is provided with a hardware monitor (LM87). This device is capable to observe the board and on-board memory temperatures, as well as several supply voltage rails with a resolution of 8 bit. The following table shows the mapping of the voltage inputs of the LM87 to the corresponding supply voltages of the PC5-LARGO:

Input	Source	Resolution [mV]	Register
AIN1	Processor Core Voltage	9.8	0x28
AIN2	+1.5V	9.8	0x29
VCCP1	+1.35V DDR Voltage	14.1	0x21
VCCP2/D2-	+1.8V	14.1	0x25
+2.5V/D2+	+1.05V	13	0x20
+3.3V	+3.3V	17.2	0x22
+5V	+5V	26	0x23
+12V	+10V	62.5	0x24

Beside the continuous measuring of temperatures and voltages the LM87 may compare these values against programmable upper and lower boundaries. As soon as a measurement violates the allowed value range, the LM87 can request an interrupt via the GPI13 input of the QM87 PCH (which may result in a system management interrupt).

Board Control and Status Registers (BCSR)

A set of board control and status registers allow to program special features on the PC5-LARGO:

- Assert a full reset
- Control activity of front panel reset and power event button
- Program time-outs and trigger a watchdog
- Get access to two LEDs in the front panel
- Get power fail and watchdog status of last board reset

The register set consists of five registers located on the SMBus at Device ID=0x5c on the following addresses:

- 0xA0: CMD_CTRL0_WR: Write to Control Register 0 (Write-Only)
- 0xA1: CMD_CTRL0_RD: Read from Control Register 0 (Read-Only)
- 0xB0: CMD_STAT0_WR: Write to Status Register 0 (Write-Clear)
- 0xB1: CMD_STAT0_RD: Read from Status Register 0 (Read-Only)
- 0xB2: CMD_STAT1_WR: Write to Status Register 1 (Write-Clear)
- 0xB3: CMD_STAT1_RD: Read from Status Register 1 (Read-Only)
- 0xC1: CMD_PLDREV_RD: Read from PLD Revision Register (Read-Only)

To prevent misfunction accesses to the registers should be done by SMBus “Byte Data” commands. Further writes to read-only or reads to write-only registers should be omitted.

Write/Read Control Register 0

Write: SMBus Address 0xA0
Read: SMBus Address 0xA1

Default after reset: 0x00

Bit	Description CMD_CTRL0
7	**GPLED** 0=Green part of the front panel LED GP is off (Default) 1=Green part of the front panel LED GP is on
6	**FPDIS** 0=Enable the front panel handle switch (Default) 1=Disable the front panel handle switch
5	**FERP#** 0=The front panel handle switch generates a power event (Default) 1=The front panel handle switch generates a system reset
4:3	**WDGT0:WDGT1** Maximum Watchdog retrigger time: 0:0 2 sec 1:0 10 sec 0:1 50 sec 1:1 250 sec
2	**WDGTRG** Retrigger Watchdog. Any change of this bit will retrigger the watchdog. After a system reset the watchdog is in an inactive state. The watchdog is armed on the 1st edge of this bit.
1	**PGLED** 0=Red part of the front panel LED PG is off (Default) 1=Red part of the front panel LED PG is blinking
0	**SRES** 0=Normal operation (Default) 1=A full system reset is performed

Read/Clear Status Register 0

Write: SMBus Address 0xB0
Read: SMBus Address 0xB1

Bit	Description CMD_STAT0
7	**PF18S** 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.8S voltage regulator
6	**PF15S** 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.5S voltage regulator
5	**PF135S** 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.35S voltage regulator
4	**RESERVED** Always read as 0
3	**PF105M** 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.05M voltage regulator
2	**PF105S** 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.05S voltage regulator
1	**RESERVED** Always read as 0
0	**PFVRC** 0=Normal operation 1=Last system reset may be caused by a power failure of the CPU voltage regulator

The bits in this register are sticky, i.e. their state will be kept even if a system reset occurs. To clear the bits a write to the register with arbitrary data may be performed.

Read/Clear Status Register 1

Write: SMBus Address 0xB2
Read: SMBus Address 0xB3

Bit	Description CMD_STAT1
7	**WDGARMD** 0=Normal operation 1=The watchdog is armed and has to be retriggered within its time-out period
6	**WDGRST** 0=Normal operation 1=Last system reset may be caused by a watchdog time-out
5	**WDGHT** 0=Normal operation 1=The watchdog already has elapsed half of its time-out period
4	**PF12A** 0=Normal operation 1=Power failure on the +12V voltage rail
3	**PF5S** 0=Normal operation 1=Last system reset may be caused by a power failure of the +V5S voltage regulator
2	**PF33M** 0=Normal operation 1=Last system reset may be caused by a power failure of the +V3.3M voltage regulator
1	**PF33A** 0=Normal operation 1=Last system reset may be caused by a power failure of the +V3.3A voltage regulator
0	**PF33S** 0=Normal operation 1=Last system reset may be caused by a power failure of the +V3.3S voltage regulator

Except of WDGHT and WDGARMD the bits in this register are sticky, i.e. their state will be kept even if a system reset occurs. To clear the bits a write to the register with arbitrary data may be performed.

Read PLD Revision Register

Write: Not allowed

Read: SMBus Address 0xC1

Bit	Description CMD_PLDREV
7:0	**PLDREV** Read PLD Revison Number

GPIO Usage

GPIO Usage QM87 PCH

GPIO Usage QM87 PCH				
GPIO	Type	Voltage [1)]	Function	Description
0	I	+V3.3S	THRM_ALERT#	Monitoring of processor PROCHOT#
1	I	+V3.3S	EXP_SMI#	Expansion Interface SMI Request (P-EXP Pin 15)
2	I	+V3.3S	CPCI_INTP	CompactPCI Interrupt Request Line CPCI_INTP
3	I	+V3.3S	CPCI_ENUM#	CompactPCI System Enumeration Line ENUM#
4	I	+V3.3S	CPCI_PS_FAL_ON#	CompactPCI Power Failure Line CPCI_FAL#/PS_ON#
5	I	+V3.3S	PM_MEMTS#	Memory Thermal Sensor Event
6	I	+V3.3S	N/A	Not used on PC5 (pulled via resistor to GND)
7	I	+V3.3S	GP_JUMP#	Reset UEFI BIOS Setup to Factory Defaults, Jumper J-GP
8	O	+V3.3A	CPCI_SYSEN_#	Sense CompactPCI® System Slot Enable Line SYSEN#
9	I	+V3.3A	USB_OC5#	USB P-HSE Port 2 Overcurrent Detect
10	I	+V3.3A	USB_OC6#	USB P-HSE Port 3 or 4 Overcurrent Detect
11	I	+V3.3A	NV-GP1	Non-Volatile Jumper
12	O	+V3.3A	NC1_ENABLE	Enable Ethernet Controller NC1
13	I	+V3.3A	HM_INT#	Hardware Monitor LM87 Interrupt Line
14	I	+V3.3A	USB_OC7#	USB P-EXP Port 1 or 2 Overcurrent Detect
15	O	+V3.3A	N/A	Not connected on PC5
16	O	+V3.3S	SE_SYS_WP	General Purpose Serial EEPROM Write Protection
17	I	+V3.3S	PPSM_EN	Connect IEEE 1588 PPS/PPM to J-GP and CompactPCI® J2 LOW: PPS/PPM disconnected from J-GP and J2 HIGH: PPS/PPM connected to J-GP and J2
18	O	+V3.3S	GP_LED_RED	General Purpose Red LED Control (via PLD)
19	I	+V3.3S	N/A	One of the Config Straps for boot device selection, pulled to +V3.3S..
20	I	+V3.3S	PCIE_CLK_REQ2#	CompactPCI® PlusIO Clock Request (CLKOE_4J2#)
21	I	+V3.3S	N/A	Not used on PC5 (pulled via resistor to GND)
22	O	+V3.3S	SGPIO_CLOCK	CompactPCI PLusIO GPIO Bus CLOCK (J2_ SATA_SCL)
23	I	+V3.3S	N/A	Not connected on PC5
24	O	+V3.3A	USB_POWEN1#	USB Front Panel Right Port Power Enable
25	I	+V3.3A	PCIE_CLK_REQ3#	CompactPCI® PlusIO Clock Request (CLKOE_1J2#)
26	I	+V3.3A	PCIE_CLK_REQ4#	Clock Request received from internal PCIe Switch
27	I	+V3.3A	NC1_WAKE#	Ethernet Controller NC1 WAKE#
28	O	+V3.3A	USB_POWEN2#	USB Front Panel Left Port Power Enable

GPIO Usage QM87 PCH				
GPIO	Type	Voltage [1)]	Function	Description
29	O	+V3.3A	N/A	Not connected on PC5
30-31	I	+V3.3A	N/A	Not used on PC5 (pulled via resistors to +3.3V)
32	I	+V3.3S	N/A	Not used on PC5 (pulled via resistor to +3.3V)
33	O	+V3.3S	N/A	Not connected on PC5
34	O	+V3.3S	EXP_SMB_EN	Connect SMBus on P-EXP to local SMBus LOW: P-EXP disconnected from SMBus HIGH: P-EXP connected to SMBus
35	O	+V3.3S	CPCI_SMB_EN	Connect SMBus on CompactPCI PlusIO to local SMBus LOW: CPCI Backplane disconnected from SMBus HIGH: CPCI Backplane connected to SMBus
36	I	+V3.3S	N/A	Not used on PC5 (pulled via resistor to GND)
37	I	+V3.3S	N/A	Not used on PC5 (pulled via resistor to +3.3V)
38	O	+V3.3S	SGPIO_LOAD	CompactPCI PlusIO GPIO Bus LOAD (J2_SATA_SCL)
39	O	+V3.3S	SGPIO_OUT	CompactPCI PlusIO GPIO Bus DATAOUT (J2_SATA_SDO)
40	I	+V3.3A	USB_OC1#	USB Front Panel Left Port Overcurrent Detect
41	O	+V3.3A	ENABLE_NC3	Enable Ethernet Controller NC3
42	O	+V3.3A	ENABLE_NC4	Enable Ethernet Controller NC4
43	I	+V3.3A	USB_OC4#	USB P-HSE Port 1 Overcurrent Detect
44	I	+V3.3A	PCIE_CLK_REQ5#	CompactPCI® PlusIO Clock Request (CLKOE_3J2#)
45	I	+V3.3A	PCIE_CLK_REQ6#	CompactPCI® PlusIO Clock Request (CLKOE_2J2#)
46	I	+V3.3A	PCIE_CLK_REQ7#	Clock Request received from PCIe to PCI bridge for J1
47	I	+V3.3A	PEG_A_CLK_RQ#	Clock Request received from PCIe clock buffer
48	I	+V3.3S	CPCI_INTS_EN	LOW: Isolate SERIRQ from CPCI_INTS HIGH: Connect SERIRQ to CPCI_INTS
49	I	+V3.3S	N/A	Not used on PC5 (pulled via resistors to GND)
50	I	+V3.3S	HWREV	PCB Revision Code HWREV[2:0]: GPIO[54/52/50] 000 001 010 ... 111 Revision 0 1 2 ... 7
51	O	+V3.3S	N/A	One of the Config Straps for boot device selection, pulled to +V3.3S.
52	I	+V3.3S	N/A	PCB Revision Code HWREV[2:0], see GPIO50
53	O	+V3.3S	N/A	Not connected on PC5
54	I	+V3.3S	N/A	PCB Revision Code HWREV[2:0], see GPIO50
55	O	+V3.3S	ENABLE_NC2	Enable Ethernet Controller NC2
56	I	+V3.3A	N/A	Not used on PC5 (pulled via resistor to GND)
57	I	+V3.3A	N/A	TPM2.0 Physical Present Pin

GPIO Usage QM87 PCH				
GPIO	Type	Voltage [1)]	Function	Description
58	I	+V3.3A	N/A	Not used on PC5 (pulled via resistor to +3.3V)
59	I	+V3.3A	USB_OC0#	USB Front Panel Right Port Overcurrent Detect
60	I	+V3.3A	N/A	Not used on PC5 (pulled via resistor to +3.3V)
61-62	O	+V3.3A	N/A	Not connected on PC5
63	O	+V3.3A	SLP_S5#	Multiplexed with chipset internal function
64	O	+V3.3S	CLKOUT_FLEX1	14.318MHz Clock Source
65-67	O	+V3.3A	N/A	Not connected on PC5
68-71	I	+V3.3S	BOARD_CFG	Board Configuration Jumpers BOARD_CGF[0:3]
72	I	+V3.3A	N/A	Not used on PC5 (pulled via resistor to +3.3V)
73	I	+V3.3A	PCIE_CLK_REQ0#	Ethernet Controller NC1 Clock Request
74-75	I	+V3.3A	N/A	Not used on PC5 (pulled via resistors to +3.3V)

[1)] S=Core Voltage (active in state S0 only), A=Standby Voltage

Configuration Jumpers

Configuration PCI Express Switch (DS-P)

The link width and transfer rate of the PCI Express interfaces attached to the local expansion connector P-PCIE is configurable by two DIP switches (DS-P) located on the backside of the PC5-LARGO. Note that changes in PCIe link configuration are honoured by the board not before a system reset was performed.

DS-P

DS-P		PCIe Link Width	
1	2	PCIe Switch Upstream	P-PCIE
OFF	OFF	4 Lanes @ 5GT/s	4 Links x 1 Lane @ 5GT/s
ON	OFF	4 Lanes @ 5GT/s	1 Link x 4 Lanes @ 5GT/s
OFF	ON	4 Lanes @ 2.5GT/s	4 Links x 1 Lane @ 2.5GT/s
ON	ON	4 Lanes @ 2.5GT/s	1 Link x 4 Lanes @ 2.5GT/s

[1)] Consists to the non fat pipe slots, generally periphery slots 3 to 8.

When the port on P-PCIE is configured as single link, the PCIe switch may size down the link width to x2 or x1 by auto-negotiation.

The following table shows the factory settings of DS-P with different side boards mounted to the PC5-LARGO:

Side Board	DS-P		PCIe Link Width
	1	2	P-PCIE
None	OFF	OFF	4 Links x 1 Lane @ 5GT/s
CCI-RAP	OFF	OFF	4 Links x 1 Lane @ 5GT/s
CCK-MARIMBA	ON	OFF	1 Link x 4 Lanes @ 5GT/s
CCL-CAPELLA	ON	OFF	1 Link x 4 Lanes @ 5GT/s
PCS-BALLET	OFF	OFF	4 Links x 1 Lane @ 5GT/s
SCS-TRUMPET	OFF	OFF	4 Links x 1 Lane @ 5GT/s

Loading UEFI BIOS Setup Defaults/IEEE 1588 Pulse per Second (J-GP)

The jumper J-GP may be used to reset the UEFI BIOS configuration settings to a default state. The UEFI BIOS on PC5-LARGO stores most of its settings in an area within the BIOS flash, e.g. the actual boot devices. Using the jumper J-GP is only necessary, if it is not possible to enter the setup of the BIOS. To reset the settings mount a jumper on J-GP and perform a system reset. As long as the jumper is stuffed the BIOS will use the default configuration values after any system reset. To get normal operation again, the jumper has to be removed.

There is also an alternate function available on J-GP. Pin 1 of this jumper carries a Pulse per Second (PPS) signal according the IEEE 1588 specification when enabled by UEFI BIOS settings. A wire may be connected to trigger events on external devices.

NOTE: The PPS signal can be gripped at the CompactPCI® PlusIO connector J2 pin D14 (SATA-SCL) also.

J-GP

J-GP	Function
Jumper Removed [1)]	Normal operation
Jumper Installed	BIOS configuration reset performed

[1)] This setting is the factory default

Manufacturer Mode Jumper (J-MFG)

The jumper J-MFG is used to bring the board into the manufacturer mode. This is necessary only on board production time and should not used by customers. For normal operation the jumper should be removed. The pin header J-MFG is not stuffed on the PC5-LARGO by default.

J-MFG

J-MFG	Function
Jumper Removed [1)]	Normal operation
Jumper Installed	Entering Manufacturer Mode

[1)] This setting is the factory default

RTC Reset (J-RTC)

The jumper J-RTC may be used to reset certain register bits of the battery backed RTC core within the PCH QM87. This can be necessary under rare conditions (e.g. battery undervoltage), if the CPU fails to enter the BIOS POST after power on. Note that installing of jumper J-RTC will neither set UEFI BIOS Setup to EKF Factory Defaults nor resets the time and date register values of the RTC (Real Time Clock). To reset the RTC core the board must be removed from the system rack. Short-circuit the pins of J-RTC for about 1 sec. Thereafter reinstall the board to the system and switch on the power. It is important to accomplish the RTC reset while the board has no power. The pin header J-RTC is not stuffed on the PC5-LARGO by default.

J-RTC

J-RTC	Function
Jumper Removed [1)]	Normal operation
Jumper Installed	RTC reset performed

[1)] This setting is the factory default.

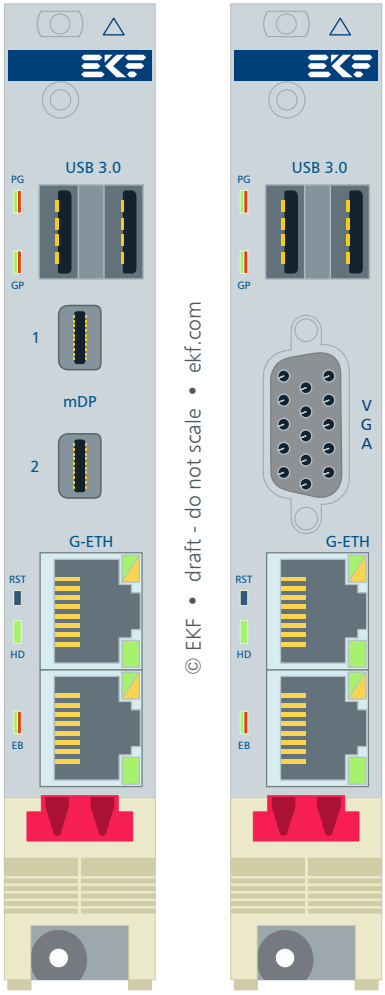
Connectors

Caution

Some of the internal connectors provide operating voltage (3.3V, 5V and 12V) to devices inside the system chassis, such as internal peripherals. Not all of these connectors are short circuit protected. Do not use these internal connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the board, the interconnecting cable and the external devices themselves.

Front Panel Connectors

With respect to the video connector, the PC5-LARGO is available in two flavours, either dual mDP or VGA.

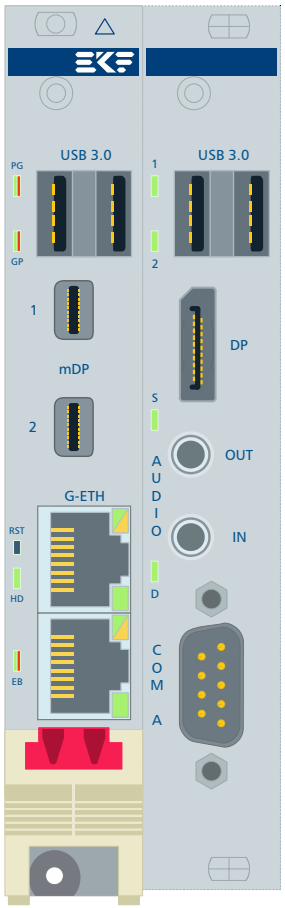


PC5-LARGO
Dual - mDP

PC5-LARGO
VGA

Sample Front Panel Options 8HP

1



PC5-LARGO
Dual - mDP

PCS-BALLET
RS-232

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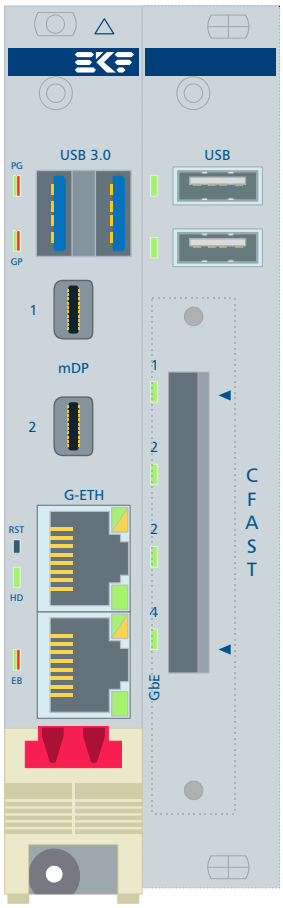
2



PC5-LARGO
Dual - mDP

PCL-CAPELLA
CFast™

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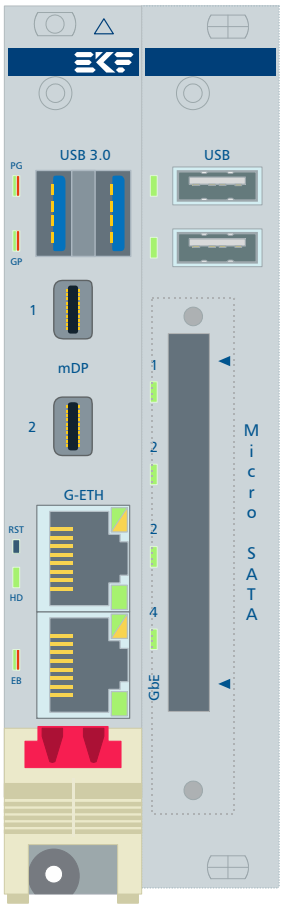
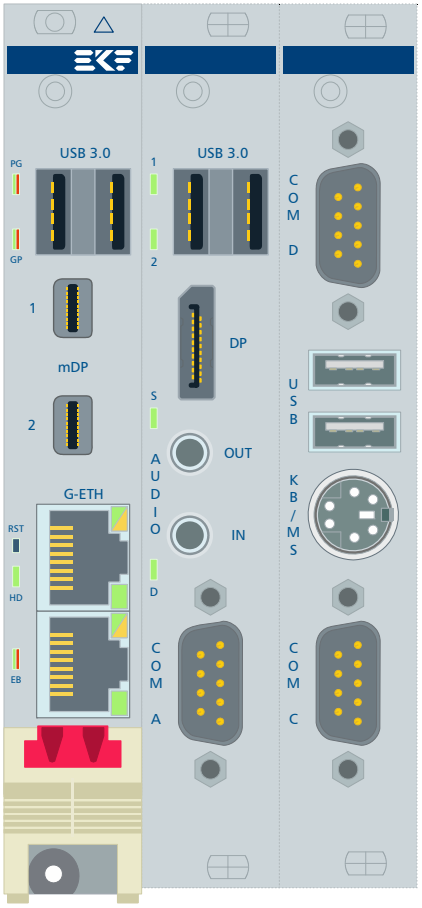


PC5-LARGO
Dual - mDP

PCL-CAPELLA
μ SATA

Sample Front Panel Options 12HP

3



PC5-LARGO
Dual - mDP

PCS-BALLET
RS-232

C32-FIO

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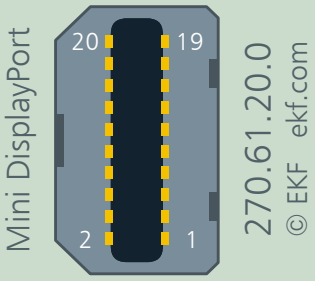
DisplayPort Connectors

The Intel® Core™ processors used on PC5-LARGO are equipped with an integrated graphics controller, which supports DisplayPort interfaces permitting simultaneous independent operation of up to three displays. Two DP receptacles are available from the PC5-LARGO front panel, as mDP (Mini DisplayPort) connectors, which is a space saving alternate to the standard DP connector and is also specified by the VESA.



Mini DisplayPort P-DP1/2				
	20	PWR [1]	19	GND
	18	AUX_CH(N)	17	LANE2(N)
	16	AUX_CH(P)	15	LANE2(P)
	14	GND	13	GND
	12	LANE3(N)	11	LANE1(N)
	10	LANE3(P)	9	LANE1(P)
	8	GND	7	GND
	6	CONFIG2 (GND)	5	LANE0(N)
	4	CONFIG1	3	LANE0(P)
	2	Hot Plug Detect	1	GND

[1] +3.3V via 0.5A current-limited electronic power switch. This voltage is switched on in S0 state only.

Most DisplayPort monitors come with the standard DP connector, hence requiring a mDP to DP cable assembly for use with the PC5-LARGO. For attachment of either a classic style analog RGB monitor, DVI or HDMI type display to the P-DP1/2 receptacles, there are both adapters and also adapter cables available.

Specified by the VESA DisplayPort connector standard is a dedicated power pin 20 (+3.3V 0.5A). Both the GPU (source side) and a DP monitor (sink side) must provide power via this pin. A VESA specified standard DisplayPort cable however should not connect the pins 20 of both cable ends, in order to avoid a back driving conflict. Fortunately the PC5-LARGO takes care about this situation. Nevertheless, before ordering DP cable assemblies, EKF recommends to verify the associated wiring diagram.

Sample VESA Compliant Mini DisplayPort Cable Assemblies EKF Part. #270.66.2.02.0	
Astron	T2M2M20020-R
Molex	0687850003
Roline	1045636
Wieson	G9858

Screw Locking Option for mDP Connectors

Opposite to the Standard DisplayPort cable connectors, mDP connectors are not provided with a latching device. For rugged applications with need for a connector locking mechanism, EKF offers two methods of fixing.

Option Screw-Lock Plate for mDP Cable Connectors

1. The front panel is provided with a threaded hole for fixing a removable H-shape retainer plate, which is available from EKF as accessory (image above).

2. As an alternate, the customer can use cable assemblies with screw-locked mDP connectors (image below). The front panel has to be modified however for this solution (two threaded holes in addition, please specify when ordering).

Screw-Locked mDP Connector Cable Assembly (Delock)

A third DisplayPort video output is available when combining the PC5-LARGO with the mezzanine side card SCS-TRUMPET or PCS-BALLET. The standard DP connector provided on these side cards is provided with latches, which may be preferred for some applications.

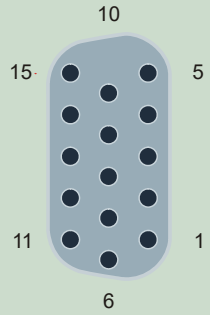
PC5-LARGO w. SCS-TRUMPET

PC5-LARGO w. PCS-BALLET Side Card & 2.5-Inch SSD, 8HP

PC5-LARGO w. PCS-BALLET C32-FIO C20-SATA, 12HP

VGA Video Connector

As an option, the PC5-LARGO can be equipped with a legacy VGA connector (High-Density D-Sub 15-position female connector). The connector VGA replaces the two Mini DisplayPort receptacles, and the digital video interface therefore is not available concurrently with this option.

P-VGA (Option)		
	1	RED
	2	GREEN
	3	BLUE
	4	NC
	5	GND
	6	GND
	7	GND
	8	GND
	9	DDC_POW [1)]
	10	GND
	11	NC
	12	VGA_DDC_SDA
	13	HSYNC
	14	VSYNC
	15	VGA_DDC_SCL

[1)] +3.3V protected by a self resetting PolySwitch fuse 0.75A. This voltage is switched on in S0 state only.

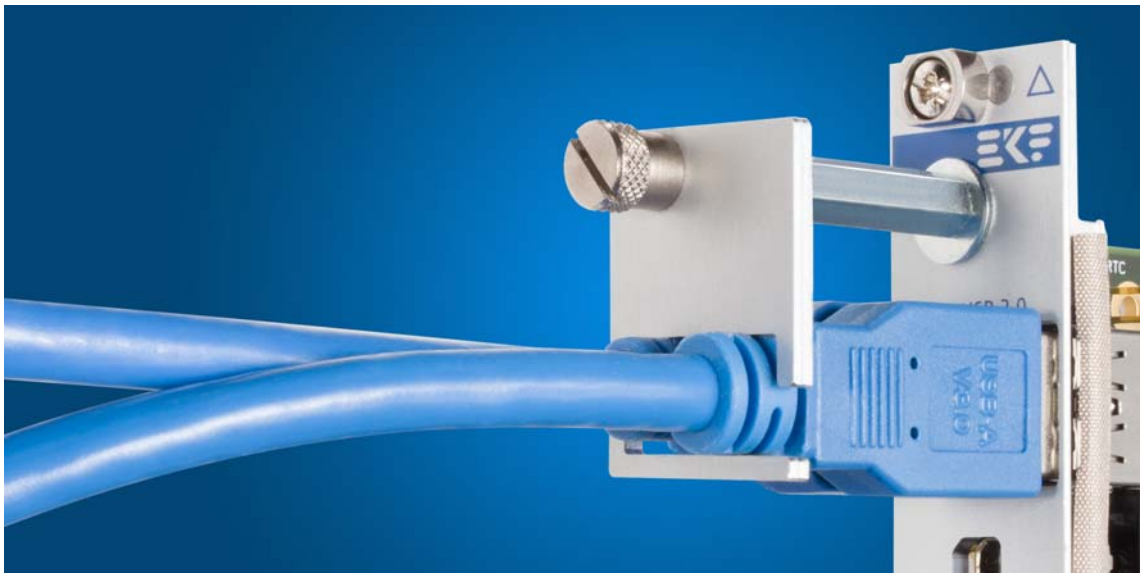
USB Connectors

The Intel® QM87 Platform Controller Hub incorporates a four-port USB 3.0 xHCI host controller. Two ports are directly available on the PC5-LARGO front panel (type A receptacle), for attachment of external USB devices.

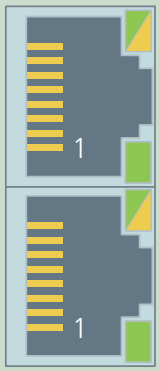
P-USB • Dual USB 3.0 Receptacle USB 3.0 dual type A receptacle, stacked, 18-position		
#270.23.18.2 © EKF • ekf.com USB 3.0 1 2	1	VBUS +5V, 1.5A max [1]
	2	USB D-
	3	USB D+
	4	GND
	5	SS RX-
	6	SS RX+
	7	GND
	8	SS TX-
	9	SS TX+

[1] +5V via 1.5A current-limited electronic power switch. Power rail may be switched off by software independently for each port.

Another two USB 3.0 connectors would be available when the PC5-LARGO is combined with the PCS-BALLET mezzanine side card. EKF offers USB cable connector retainer solutions, for rugged applications (picture below).



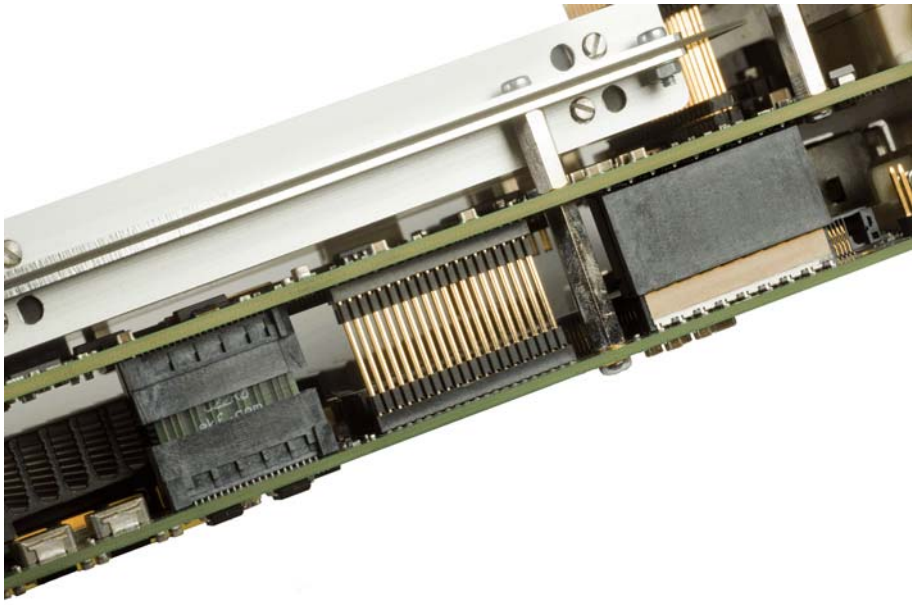
Ethernet Connectors

Gigabit Ethernet Ports 1/2 (P-ETH, RJ-45)			
 270.02.08.5	Port 1 iAMT	1	NC1_MDX0+
		2	NC1_MDX0-
		3	NC1_MDX1+
		4	NC1_MDX2+
		5	NC1_MDX2-
		6	NC1_MDX1-
		7	NC1_MDX3+
		8	NC1_MDX3-
	Port 2 IEEE 1588	1	NC2_MDX0+
		2	NC2_MDX0-
		3	NC2_MDX1+
		4	NC2_MDX2+
		5	NC2_MDX2-
		6	NC2_MDX1-
		7	NC2_MDX3+
		8	NC2_MDX3-

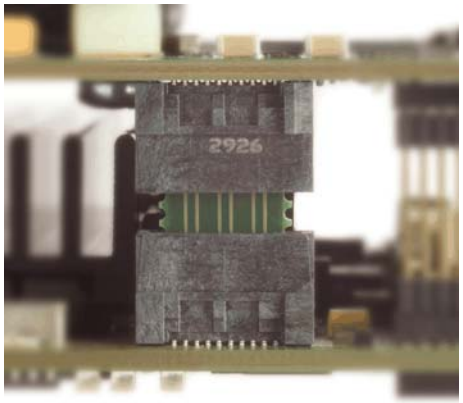
The lower green LED indicates LINK established when continuously on, and data transfer (activity) when blinking. If the lower green LED is permanently off, no LINK is established. The upper green/yellow dual-LED signals the link speed 1Gbit/s when lit yellow, 100Mbit/s when lit green, and 10Mbit/s when off.

Mezzanine Connectors

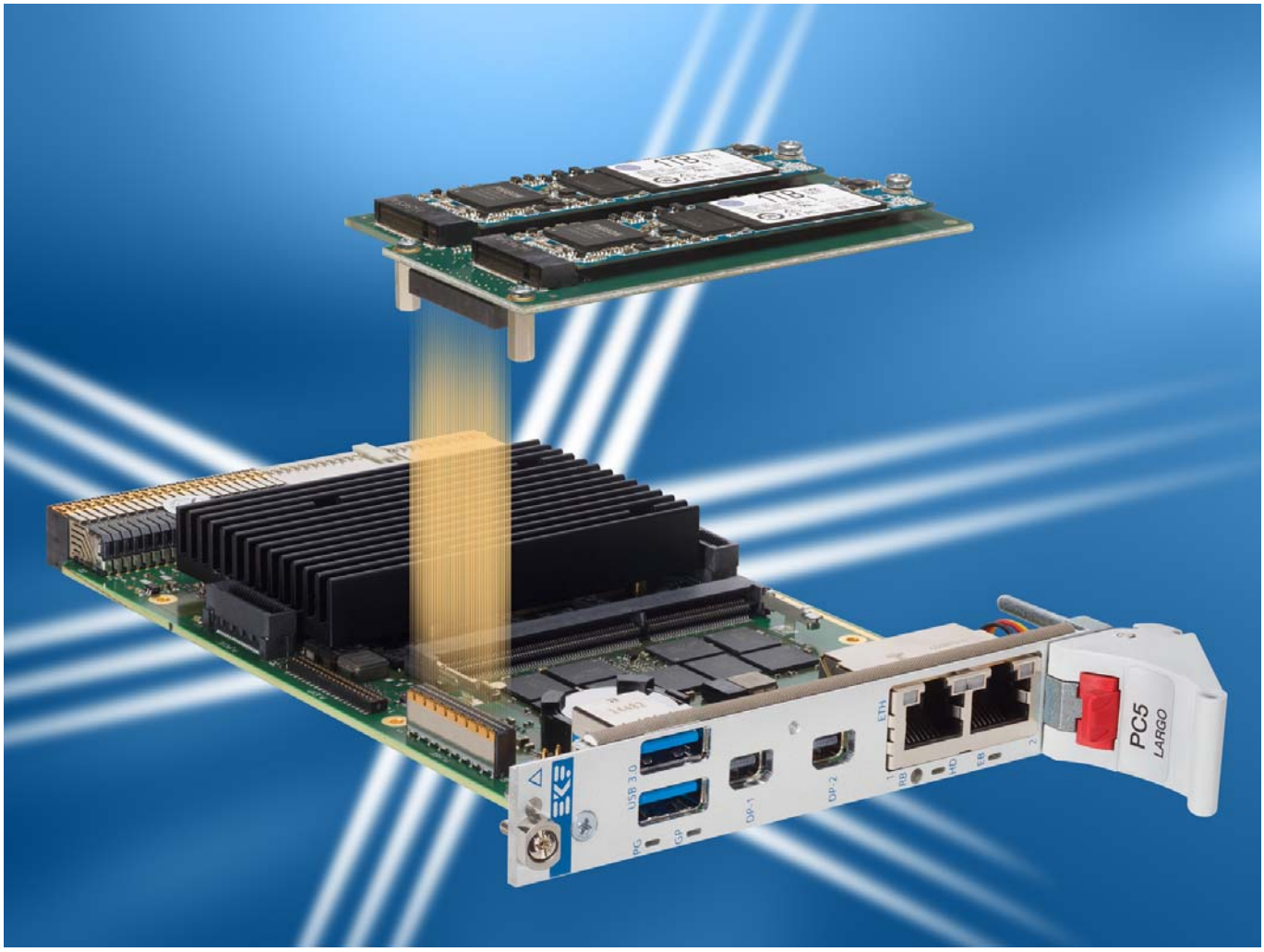
Mezzanine Side Card Connector Suite (Picture Similar)



PCIE EXP HSE

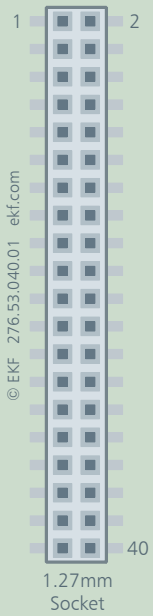


DP



PC5-LARGO w. Low Profile Mezzanine Modul HSE Connector Based

Expansion Interface P-EXP

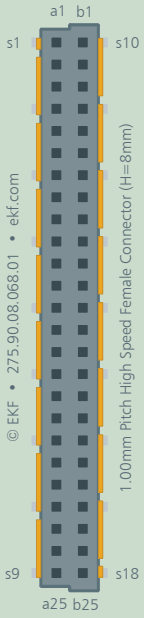


P-EXP			
GND	1	2	+3.3V [1]
PCI_CLK (33MHz)	3	4	RST_PLC#
LPC_AD0	5	6	LPC_AD1
LPC_AD2	7	8	LPC_AD3
LPC_FRM#	9	10	LPC_DRQ#
GND	11	12	+3.3V [1]
LPC_SERIRQ	13	14	WAKE#
EXP_SMI#	15	16	SIO_CLK (14.3MHz)
FWH_ID0	17	18	FWH_INIT#
KBRST#	19	20	A20GATE
GND	21	22	+5V [1]
USB_EXP2-	23	24	USB_EXP1-
USB_EXP2+	25	26	USB_EXP1+
USB_EXP_OC#	27	28	DBRESET#
EXP_SCL [2]	29	30	EXP_SDA [2]
GND	31	32	+5V [1]
HDA_SDOUT	33	34	HDA_SDIN0
HDA_RST#CL_RST# [3]	35	36	HDA_SYNC
HDA_CLK/CL_CLK [3]	37	38	HDA_SDIN1/CL_DATA [3]
SPEAKER	39	40	+12V [4]

[1] Power rail switched on in state S0 only.
[2] Connected to SMBus via buffered switch, isolated after reset.
[3] Stuffing option, default is the HDA option.
[4] Power rail switch off in state S5.

WARNING: The +3.3V, +5V and +12V power pins are not protected against a short circuit event. The connector P-EXP therefore should be used only for attachment of an approved expansion side card. The maximum current flow across these pins should be limited to 1A per power pin.

High Speed Expansion Connector P-HSE



High Speed Expansion P-HSE			
GND	a1	b1	GND
SATA_HSE1_TXP	a2	b2	SATA_HSE3_TXP
SATA_HSE1_TXN	a3	b3	SATA_HSE3_TXN
GND	a4	b4	GND
SATA_HSE1_RXN	a5	b5	SATA_HSE3_RXN
SATA_HSE1_RXP	a6	b6	SATA_HSE3_RXP
GND	a7	b7	GND
SATA_HSE2_TXP	a8	b8	SATA_HSE4_TXP
SATA_HSE2_TXN	a9	b9	SATA_HSE4_TXN
GND	a10	b10	GND
SATA_HSE2_RXN	a11	b11	SATA_HSE4_RXN
SATA_HSE2_RXP	a12	b12	SATA_HSE4_RXP
GND	a13	b13	GND
USB_HSE1_P	a14	b14	USB_HSE3_P
USB_HSE1_N	a15	b15	USB_HSE3_N
GND	a16	b16	GND
USB_HSE2_P	a17	b17	USB_HSE4_P
USB_HSE2_N	a18	b18	USB_HSE4_N
GND	a19	b19	GND
USB_HSE_OC1#	a20	b20	USB_HSE_OC34#
USB_HSE_OC2#	a21	b21	USB_HSE_OC34#
+3.3VS [1)]	a22	b22	+5VS [1)]
+3.3VS [1)]	a23	b23	+5VS [1)]
+3.3VA [2)]	a24	b24	+5VA [2)]
+12V [3)]	a25	b25	+12V [3)]

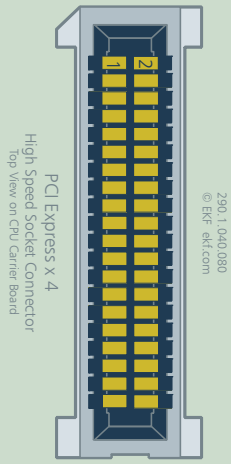
1) Power rail switched on in state S0 only (Switched).
2) Power rail on with system stand-by power (Always).
3) Power rail switch off in state S5.
4) All SATA channels are derived from the PCH QM87.
5) All TX/RX designations with respect to the SATA controller.

WARNING: The +3.3V, +5V and +12V power pins are not protected against a short circuit event. The connector P-HSE therefore should be used only for attachment of an approved expansion side card. The maximum current flow through these power pins should be limited to 0.5A per pin.

C47-MSATA Mezzanine Storage Module Based on the Connector HSE

C48-M2 Mezzanine Storage Module Based on the Connector HSE

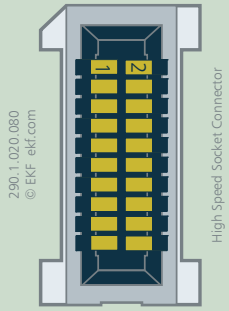
PCI Express® Expansion Header P-PCIE

P-PCIE				
	GND	1	2	GND
	+5V [1]	3	4	+3.3V [1]
	+5V [1]	5	6	+3.3V [1]
	GND	7	8	GND
	PE_CLKP	9	10	PLTRST#
	PE_CLKN	11	12	PE_WAKE#
	GND	13	14	GND
	PE_1TP	15	16	PE_1RP
	PE_1TN	17	18	PE_1RN
	GND	19	20	GND
	GND	21	22	GND
	PE_2TP	23	24	PE_2RP
	PE_2TN	25	26	PE_2RN
	GND	27	28	GND
	PE_3TP	29	30	PE_3RP
	PE_3TN	31	32	PE_3RN
	GND	33	34	GND
	PE_4TP	35	36	PE_4RP
	PE_4TN	37	38	PE_4RN
	GND	39	40	GND

[1] Power rail switched on in state S0 only.

WARNING: The +3.3V and +5V power pins are not protected against a short circuit event. The connector P-PCIE therefore should be used only for attachment of an approved expansion side card. The maximum current flow through these power pins should be limited to 1A per pin.

DisplayPort Expansion Header P-DP3

P-DP3				
	GND	1	2	GND
	DP_LANE0+	3	4	DP_LANE3+
	DP_LANE0-	5	6	DP_LANE3-
	GND	7	8	GND
	DP_LANE1+	9	10	DP_AUX+
	DP_LANE1-	11	12	DP_AUX-
	GND	13	14	GND
	DP_LANE2+	15	16	DP_HPD
	DP_LANE2-	17	18	DP_CFG1
	GND	19	20	GND

Pin Headers & Debug

Front Panel Handle Microswitch Header P-FPH

The jumper P-FPH is used for attachment of an external SPDT switch. By default, P-FPH is connected across a short cable harness to a microswitch, which is integrated into the PC5-LARGO front panel handle (ejector lever). The switch performs a power button event (e.g. system shutdown) by short-circuiting the pins 1 and 3 of P-FPH when activated (hold unlock button of front panel handle depressed momentarily).

P-FPH		
# 276.02.003.11 © EKF • ekf.com 		
1	black	Microswitch Pole (Common), Wired to PLD
2	red	Microswitch Throw - F/P Handle Locked Position, NC
3	yellow	Microswitch Throw - F/P Handle Unlocked Position, Wired to GND

PLD Programming Header P-ISP

The PC5-LARGO is provided with a powerful PLD (in-System Programmable Logic Device) which replaces legacy glue logic. The programming header P-ISP is not stuffed (in use for manufacturing only). Its footprint is situated at the bottom side of the board.

P-ISP

1	+3.3V
2	TDO
3	TDI
4	*NC*
5	*KEY*
6	TMS
7	GND
8	TCK

Processor Debug Header P-XDP

The PC5-LARGO may be equipped with a 26-position processor debug header for hard- and software debugging (specified by Intel® as XDP-SFF-26 Pin Platform Connection). The connector is suitable for installation of a flat flex cable (FFC), in order to attach an JTAG debugger (emulator) such as the Arium ECM-XDP3. An adapter (ITP-XDP-SFF-26) is required in addition to convert the 26-pin XDP-SFF-26 Pin connector to the standard 60-pin XDP.

The header P-XDP would be mounted on the PCB bottom side, but is not stuffed by default.

P-XDP Processor Debug Connector			
269.1.026.902 • FFC Connector  © EKF • ekf.com			
1	OBSFN_A0 (PREQ#)	OBSFN_A1 (PRDY#)	2
3	GND	*OBSDATA_A0*	4
5	*OBSDATA_A1*	GND	6
7	*OBSDATA_A2*	OBSDATA_A3 (CPU_CFG3)	8
9	GND	HOOK0 (CPU_PWRGOOD)	10
11	HOOK1 (XDP_PWRBTN)	HOOK2 (PWR_DBG#)	12
13	HOOK3 (SYS_PWROK)	*HOOK4*	14
15	*HOOK5*	VCCOBS_AB (VCCIO_CPU)	16
17	HOOK6 (PLTRST#)	HOOK7 (DBRESET#)	18
19	GND	TDO	20
21	TRST#	TDI	22
23	TMS	*TCK1*	24
25	GND	TCK0 (TCK)	26

Backplane Connectors

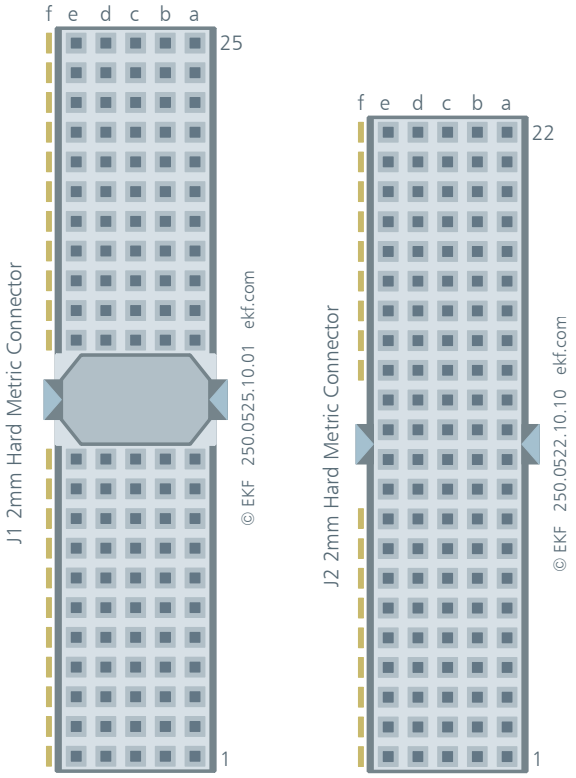
CompactPCI J1

J1	A	B	C	D	E
25	5V	*REQ64#* [2]	ENUM# [1]	3.3V	5V
24	AD1	5V	V(I/O)	AD0	*ACK64#* [2]
23	3.3V	AD4	AD3	5V	AD2
22	AD7	GND	3.3V	AD6	AD5
21	3.3V	AD9	AD8	GND/M66EN [7]	C/BE0#
20	AD12	GND	V(I/O)	AD11	AD10
19	3.3V	AD15	AD14	GND	AD13
18	SERR# [1]	GND	3.3V	PAR	C/BE1#
17	3.3V	IPMB SCL [3]	IPMB SDA [3]	GND	PERR# [1]
16	DEVSEL# [1]	GND	V(I/O)	STOP# [1]	LOCK# [1]
15	3.3V	FRAME# [1]	IRDY# [1]	BD_SEL# [6]	TRDY# [1]
14	KEY AREA				
13					
12					
11	AD18	AD17	AD16	GND	C/BE2#
10	AD21	GND	3.3V	AD20	AD19
9	C/BE3#	GND	AD23	GND	AD22
8	AD26	GND	V(I/O)	AD25	AD24
7	AD30	AD29	AD28	GND	AD27
6	REQ# [1]	GND	3.3V	CLK	AD31
5	*BRSVP1A5* [4]	*BRSVP1B5* [4]	RST#	GND	GNT#
4	IPMB PWR	GND	V(I/O)	INTP [1]	INTS [1]
3	INTA# [1]	INTB# [1]	INTC# [1]	5V	INTD# [1]
2	*TCK* [4]	5V	*TMS* [4]	*TDO* [4]	*TDI* [4]
1	5V	-12V [5]	*TRST#* [4]	+12V	5V

1) This pin is pulled up with 1kΩ to V(I/O).
2) This pin is not used on PC5-LARGO, but pulled up with 1kΩ to V(I/O).
3) This pin is pulled up with 3.0k to J1 pin A4.
4) This pin is not connected.
5) This pin is connected to a decoupling capacitor only and not used on PC5-LARGO.
6) This pin is connected to power sequencing logic and should pulled low for normal operation.
7) This pin can be pulled down on PC5-LARGO to force 33 MHz operation on request. The PC5-LARGO is capable to operate with 66 MHz on the CPCI Bus by default.

CompactPCI J2 (PlusIO)

This connector is a high speed UHM connector, suitable for Gigabit Serial I/O. Refer also to PICMG® 2.30 CompactPCI® PlusIO Specification



J2 UHM (Top)
J1 (Bottom)

Please note, that the CompactPCI® PlusIO specification refers to SATA data rates of 1.5Gbps and 3Gbps. EKF has tested successfully also 6G over the backplane with sample devices, but cannot guarantee this data rate under any condition. Other devices and other backplane brands/types in use may cause a different result. Hence, for optimum reliability, the Marvell SATA controller will be initialized for 3Gbps on all ports by default. The J2 backplane SATA 6Gbps configuration would be available however as a PC5-LARGO option on special request (altered content for the Marvell 88SE9230 attached SPI Flash). EKF recommends that customers validate their particular SATA 6G application thoroughly, since SATA channel data errors can decrease the performance considerably.

Warning: Do not operate the standard PC5-LARGO in systems with a 64-bit CompactPCI® backplane. The J2/P2 pin assignment of a 64-bit CPCI backplane differs substantially from a CompactPCI® PlusIO backplane, which will result in a short circuit situation on several pins, causing permanent damage to the PC5-LARGO. For use together with a 64-bit CompactPCI® classic backplane, special PC5-LARGO versions are available on customer request, however supporting only 32-bit peripheral cards. The use of 64-bit CompactPCI® classic peripheral boards may cause problems.

J2	A	B	C	D	E
22	*GA4* [2]	*GA3* [2]	*GA2* [2]	*GA1* [2]	*GA0* [2]
21	CLK6	GND	2_ETH_B+ *RSV*	1_ETH_D+ *RSV*	1_ETH_B+ *RSV*
20	CLK5	GND	2_ETH_B- *RSV*	1_ETH_D- *GND*	1_ETH_B- *RSV*
19	GND	GND	2_ETH_A+ *RSV*	1_ETH_C+ *RSV*	1_ETH_A+ *RSV*
18	2_ETH_D+ *BRSVP2A18*	2_ETH_C+ *BRSVP2B18*	2_ETH_A- *BRSVP2C18*	1_ETH_C- *GND*	1_ETH_A- *BRSVP2E18*
17	2_ETH_D- *BRSVP2A17*	2_ETH_C- *GND*	PRST# [1]	REQ6# [1]	GNT6#
16	4_PE_CLK- *BRSVP2A16*	2_PE_CLK+ *BRSVP2B16*	DEG# [1]	GND	reserved [2] *BRSVP2E16*
15	4_PE_CLK+ *BRSVP2A15*	2_PE_CLK- *GND*	FAL# [1] (PSON#) [6]	REQ5# [1]	GNT5#
14	3_PE_CLK- *AD35*	1_PE_CLK+ *AD34*	4_PE_CLKE# *AD33*	SATA_SCL (GPIO) *GND*	reserved [2] *AD32*
13	3_PE_CLK+ *AD38*	1_PE_CLK- *GND*	3_PE_CLKE# *V(I/O)*	SATA_SDO (GPIO) *AD37*	SATA_SL *AD36*
12	4_PE_RX00+ *AD42*	1_PE_CLKE# *AD41*	2_PE_CLKE# *AD40*	SATA_SDI [2] *GND*	4_SATA_RX+ *AD39*
11	4_PE_RX00- *AD45*	4_PE_TX00+ *GND*	4_USB2+ *V(I/O)*	4_SATA_TX+ *AD44*	4_SATA_RX- *AD43*
10	3_PE_RX00+ *AD49*	4_PE_TX00- *AD48*	4_USB2- *AD47*	4_SATA_TX- *GND*	3_SATA_RX+ *AD46*
9	3_PE_RX00- *AD52*	3_PE_TX00+ *GND*	3_USB2+ *V(I/O)*	3_SATA_TX+ *AD51*	3_SATA_RX- *AD50*
8	2_PE_RX00+ *AD56*	3_PE_TX00- *AD55*	3_USB2- *AD54*	3_SATA_TX- *GND*	2_SATA_RX+ *AD53*
7	2_PE_RX00- *AD59*	2_PE_TX00+ *GND*	2_USB2+ *V(I/O)*	2_SATA_TX+ *AD58*	2_SATA_RX- *AD57*
6	1_PE_RX00+ *AD63*	2_PE_TX00- *AD62*	2_USB2- *AD61*	2_SATA_TX- *GND*	1_SATA_RX+ *AD60*
5	1_PE_RX00- *C/BE5#*	1_PE_TX00+ 64EN#	1_USB2+ *V(I/O)*	1_SATA_TX+ *C/BE4#*	1_SATA_RX- *PAR64*
4	V(I/O)	1_PE_TX00- *BRSVP2B4*	1_USB2- *C/BE7#*	1_SATA_TX- *GND*	reserved [2] *C/BE6#*
3	CLK4	GND	GNT3#	REQ4# [1]	GNT4#
2	CLK2	CLK3	SYSEN# [3]	GNT2#	REQ3# [1]
1	CLK1	GND	REQ1# [1]	GNT1#	REQ2# [1]

1) This pin is pulled up with 1kΩ to V(I/O). Alternate pull up resistor values (e.g. 2.7kΩ for V(I/O)=+3.3V) are available on request.

2) This pin is not connected.

3) This pin is pulled up with 10kΩ to +3.3V.

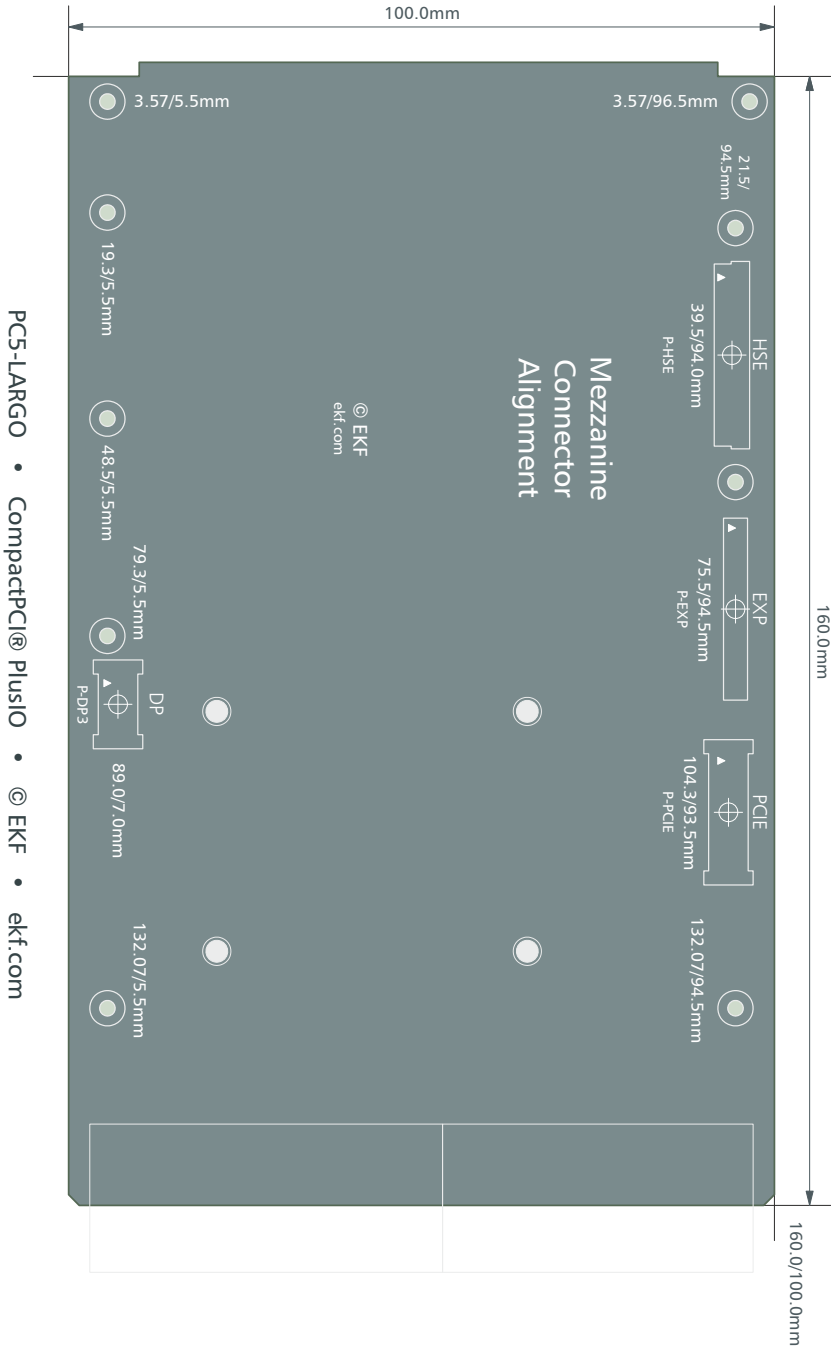
4) *Pin positions printed italic: 64-bit system slot signals (for reference only).*

5) Pin positions printed blue: PlusIO options.

6) As an exclusive stuffing option J2-C15 can be utilised as PSON# output.

Mechanical Drawing

The following drawing shows the positions of mounting holes and expansion connectors on the PC5-LARGO.



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