SYSTEM

User Guide

PC2-LIMBO • *CompactPCI® PlusIO*

Intel® Atom™ Processor E6xx Series • Low Power CPU Card

Suitable for Classic CompactPCI© and PICMG 2.30 CompactPCI® PlusIO Systems

Document No. 6240 • Edition 15 • 16 June 2016

PC2-LIMBO

Contents

About this Manual

This manual describes the technical aspects of the PC2-LIMBO, required for installation and system integration. It is intended for the experienced user only.

Edition History

Ed.	Contents/*Changes*	Author	Date
1	User Manual PC2-LIMBO, english, preliminary edition Text #6240, File: pc2_ug.wpd	jj	11 February 2011
2	Added photos PC2-LIMBO, added photos showing how to force system shutdown using the front panel handle integrated switch	jj	13 May 2011
3	BIOS usage of GP LED - document link added, photos of hybrid systems added	jj	24 May 2011
4	Added photo bottom view (microSD card holder)	jj	17 August 2011
5	Added photos PC2-C40/C43/C47	jj	22 August 2011
6	Added/changed photos front view	jj	26 August 2011
7	Major review reflecting board revision 1	mib/jj	18 January 2012
8	Chapter +5V Only Design: +3.3V power rail 15A fuse to backplane connector not populated by default. Added photos of new 44HP systems, added photos of sample hybrid backplanes	jj	4 April 2012
9	Table Feature Summary: Maxim supply current of the +3.3V power rail to backplane up to 5A	jj	26 October 2012
10	Added photos of battery options	jj	18 February 2013
11	Added photos of custom specific cooler plate. Removed VGA video option. Described SATA options more clearly. Added MTBF. Added Cfast Card recommended parts.	jj	17 April 2013
12	Replaced some photos with respect to current board revision 4, some technical details described more clearly	jj	6 August 2013
13	Added Power Requirements, P-GP function	mib	19 January 2015
14	Battery lifetime scenario	jj	8 April 2015
15	Typo corrected	jj	16 June 2016

Related Documents

Related Information PC2-LIMBO	
PC2-LIMBO Home	www.ekf.com/p/pc2/pc2.html
PC2-LIMBO Product Information	www.ekf.com/p/pc2/pc2_pi.pdf

Nomenclature

Signal names used herein with an attached '#' designate active low lines.

Trade Marks

Some terms used herein are property of their respective owners, e.g.

- Queens Bay, Tunnel Creek, Topcliff, Atom E6xx: ® Intel
- CompactPCI, CompactPCI PlusIO, CompactPCI Serial: ® PICMG
- Windows XP, Windows 7, Windows 8: ® Microsoft
- EKF, ekf system: ® EKF

EKF does not claim this list to be complete.

Legal Disclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

Standards

Reference Documents		
Term	**Document**	**Origin**
CFast™	CFast™ Specification Rev. 1.0	www.compactflash.org
CompactPCI®	CompactPCI Specification, PICMG® 2.0 R3.0, Oct. 1, 1999	www.picmg.org
CompactPCI® PlusIO	CompactPCI PlusIO Specification, PICMG® 2.30 R1.0, November 11, 2009	www.picmg.org
CompactPCI® Serial	PICMG® CPCI-S.0 (Draft as of Current)	www.picmg.org
DVI	Digital Visual Interface Rev. 1.0 Digital Display Working Group	www.ddwg.org
Ethernet	IEEE Std 802.3, 2000 Edition	standards.ieee.org
LPC	Low Pin Count Interface Specification, Revision 1.1	developer.intel.com/design/chipsets/industry/lpc.htm
microSDHC	SD Card Specifications	www.sdcard.org
HD Audio	High Definition Audio Specification Rev.1.0	www.intel.com/design/chipsets/hdaudio.htm
PCI Express®	PCI Express® Base Specification 3.0	www.pcisig.com
PCI Local Bus	PCI 2.2/2.3/3.0 Standards PCI SIG	www.pcisig.com
SATA	Serial ATA 2.5/2.6 Specification	www.sata-io.org
USB	Universal Serial Bus Specification	www.usb.org

Overview

The PC2-LIMBO is a low power 4HP/3U CompactPCI® CPU board, equipped with an Intel® Atom™ E6xx series 1.6GHz processor, available on request for the industrial operating temperature range. The PC2-LIMBO front panel is provided with two Gigabit Ethernet jacks, two USB receptacles, and a DVI video connector for attachment of a high resolution digital display.

The PC2-LIMBO is equipped with up to 2GB soldered RAM for rugged applications. An on-board CFast™ host connector is provided for attachment of a SATA SSD module. In addition, a microSD card holder can accommodate an industrial microSDHC Flash card. Further more, several SATA based low profile mass storage expansion modules are available as an option.

The PC2-LIMBO is equipped wit a set of local expansion interface connectors, which can be optionally used to attach a mezzanine side board. A variety of expansion cards is available, e.g. providing legacy I/O (e.g. RS-232) and additional PCI Express® based I/O circuitry such as SATA, USB and Gigabit Ethernet. Most mezzanine side cards can accommodate in addition a 2.5-inch drive.

Typically, the PC2-LIMBO and the related side card would come as a readily assembled 8HP unit. As an alternate, low profile mezzanine storage modules are available that fit on the PC2-LIMBO while maintaining the 4HP profile. The C42-SATA module e.g. is provided with a 1.8-Inch Micro SATA SSD up to 800GB capacity.

CompactPCI® PlusIO (PICMG 2.30) is a new standard for rear I/O across J2, specified by the PICMG®. High speed signal lines (PCI Express®, SATA, Gigabit Ethernet and USB) are passed from the PC2-LIMBO through the special UHM connector to the backplane, for usage either on a PlusIO rear I/O transition module, or CompactPCI® Serial card slots.

CompactPCI® Serial (PICMG CPCIS.0) defines a completely new card slot, based on PCI Express®, SATA, Gigabit Ethernet and USB serial data lines. On a hybrid backplane, both card styles can reside, CompactPCI® and CompactPCI® Serial, with the PC2-LIMBO in the middle as system slot controller for both backplane segments.

Technical Features

Feature Summary

Feature Summary
▸ *CompactPCI®* System Slot Controller
▸ *CompactPCI®* PlusIO Rear I/O According to PICMG® 2.30
▸ Hybrid Systems Option (Dual Backplane *CompactPCI®* & *CompactPCI® Serial*)
▸ Based on the Intel® Queens Bay Platform (Tunnel Creek CPU, Topcliff PCH)
▸ Intel® Atom™ Series E6xx Mobile Processor, Power Optimized CPU, Integrated Graphics Engine
▸ E620(T) Processor 0.6GHz 3.3W TDP (T = -40°C to +85°C)
▸ E640(T) Processor 1.0GHz 3.6W TDP (T = -40°C to +85°C)
▸ E660(T) Processor 1.3GHz 3.6W TDP (T = -40°C to +85°C)
▸ E680(T) Processor 1.6GHz 4.5W TDP (T = -40°C to +85°C)
▸ DDR2 Soldered Memory up to 2GB
▸ Integrated Graphics Controller (Front Panel: DVI Connector)
▸ Max Resolution 1920x1080
▸ Intel® EG20T (Topcliff) Platform Controller Hub (PCH)
▸ Dual Gigabit Ethernet Controllers (Individually BIOS Controlled either F/P or J2 RIO)
▸ Two Native SATA Channels 3Gbps
▸ Four Additional SATA Channels 3Gbps, Mezzanine Usage (Option on Request) and/or Rear I/O (JMicron Controllers, no BIOS Boot Support as of Current)
▸ Twelve USB 2.0 Channels
▸ CFast™ Card Host Connector on-Board (SATA 3Gbps I/F)
▸ microSD Host Connector (up to 32GB Class 6 Speed microSDHC Card Support)
▸ SATA 1.8-Inch Solid State Drive (SSD) up to 800GB with C42-SATA Mezzanine Module Option (4HP Assembly Height Maintained)
▸ CompactFlash with C40-SCFA Mezzanine Module Option (4HP Maintained)
▸ Secondary CFast™ Card Host Connector with C41-CFAST Mezzanine Module Option (4HP Maintained)
▸ On-Board PCI Express® Packet Switch (4 Lanes available for Rear I/O and CPCI Serial Backplane Respectively, another 1 Lane for Mezzanine Side Card)
▸ Legacy I/O Expansion Connectors (CAN2.0B, HD Audio, LPC, PS/2, UART)
▸ High Speed I/O Expansion Connectors (LVDS, PCI Express®, SATA, USB)
▸ Variety of Mezzanine Expansion Boards (Side Cards) Available with and w/o PCIe
▸ Most Mezzanines Optionally Equipped with 2.5-Inch Single- or Dual-Drive
▸ Rear I/O Transition Module Option (e.g. PR1-RIO)
▸ +5V Only Design, on-Board +3.3V Regulator Can Feed CPCI Peripheral Slot Cards up to 5A thus Eliminating Need for +3.3V External Power Supply Rail
▸ UEFI Phoenix BIOS with ACPI
▸ Long Term Availability
▸ Coating, Sealing, Underfilling on Request
▸ RoHS Compliant
▸ Operating Temperature 0°C to +70°C (-40°C to +85°C on Request)

Performance Rating

Performance Rating
tbd

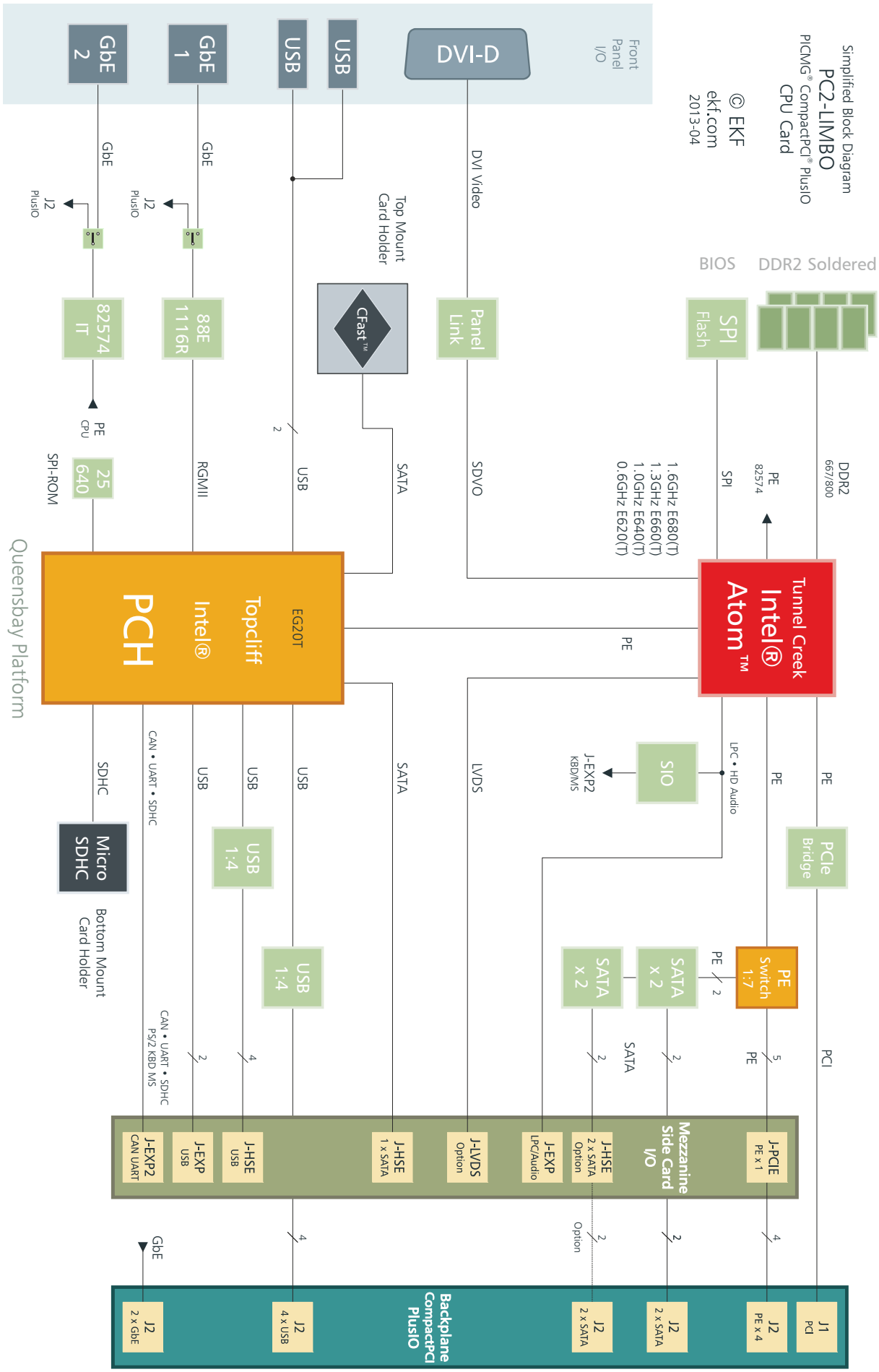
Operating Conditions

Operating Conditions	
Thermal & Environmental Conditions	▸ Operating Temperature 0°C to +70°C (-40°C to +85°C on Request) ▸ Storage temperature: -40°C to +85°C, max. Gradient 5°C/min ▸ Humidity 5% ... 95% RH non Condensing ▸ Altitude -300m ... +3000m ▸ Shock 15g 0.33ms, 6g 6ms ▸ Vibration 1g 5-2000Hz
EC Regulations	▸ EN55022, EN55024, EN60950-1 (UL60950-1/IEC60950-1) ▸ 2002/95/EC (RoHS)
MTBF	▸ 13.3 years

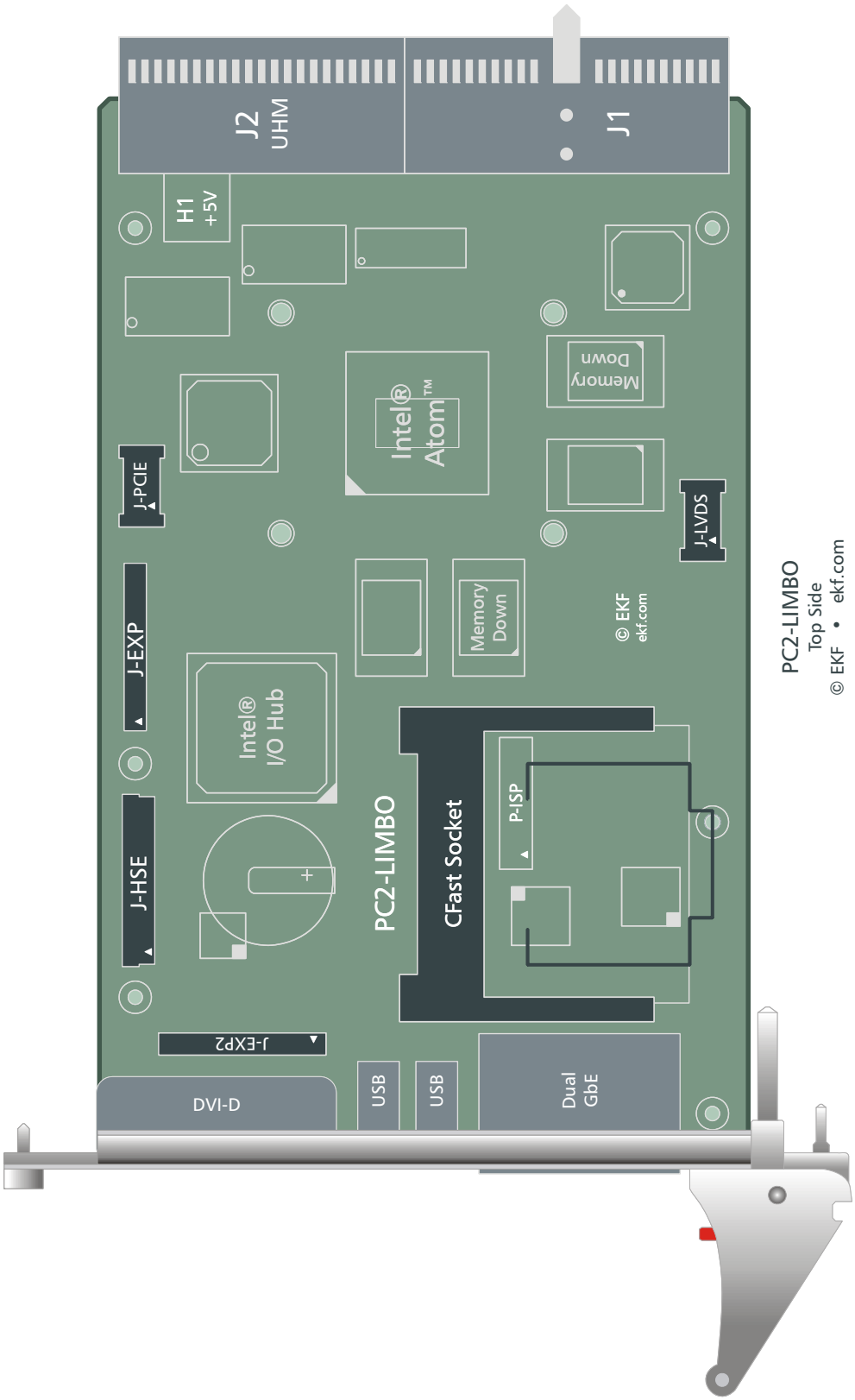
Power Requirements

Power Requirements		
		5V +0.25V/-0.15V
PC2-620D	POSReady Idle Idle	2.5A
	Power Thermal Utility 100%	2.9A
PC2-62CD	POSReady Idle Idle	1.7A
	Power Thermal Utility 100%	2.1A
PC2-41CD	POSReady Idle Idle	1.65A
	Power Thermal Utility 100%	1.85A

Block Diagram



Top View Component Assembly



Front Panel Connectors

DVI-D	DVI digital video output receptacle (DVI-I connector face for optimum compatibility with all types of DVI video cables)
ETH1/2	Dual Gigabit Ethernet RJ-45 receptacles with integrated indicator LEDs
USB1/2	Universal Serial Bus 2.0 type A receptacles

Front Panel Switches & Indicators

FPH	Front Panel Handle with integrated switch, emulates the power event button
GP	General Purpose bicolour LED
HD	LED indicating any activity on SATA ports
PG	Power Good/Board Healthy bicolour LED

On-Board Connectors & Sockets

CF1	CFast™ Card host connector (SATA SSD with CompactFlash dimensions)
H1	+5V supply power terminal block (available on request only for stand-alone applications)
J1	CompactPCI® 32-bit 33MHz standard hard metric connector
J2	CompactPCI® PlusIO Rear I/O special high speed UHM connector
J-EXP(1)	Utility EXPansion interface connector (LPC, USB, HD Audio, SMBus), available either from top (T) or bottom (B) [1)] of the board, interface to optional side board
J-EXP2	Utility EXPansion interface connector 2 (CAN2.0B, I^2C, PS/2 KB/MS, SDIO, UART), interface to optional side board. This connector is not populated by default.
J-HSE	High Speed Expansion connector (up to 4 x SATA, 4 x USB), interface to optional low profile mezzanine module or side board
J-LVDS	LVDS flat panel interface connector, interface to optional side board. This connector is not populated by default.
J-PCIE	PCI Express® expansion interface connector, interface to optional side board
MSD1	MicroSD Card holder (on the bottom side)
XDP	CPU Debug Port [1)]

[1)] Bottom connector populated on customers request only

Pin Headers

P-FPH	Pin header suitable for Front Panel Handle switch cable harness
P-ISP	PLD glue logic device programming connector, not populated

Jumpers

P-GP	Jumper to reset UEFI BIOS Setup to EKF defaults
P-RTC	Jumper to reset RTC circuitry (part of CPU), not populated

Microprocessor

The PC2-LIMBO is equipped with an Intel® Atom™ E6xx processor (code name Tunnel Creek). These low power processors provide integrated graphics and memory controller, which results in a very efficient platform design. The E6xx almost can be considered as a single-chip solution, since all functions of a typical north-bridge have been moved to the CPU, as well as some I/O circuitry of a typical south-bridge.

There is no proprietary chipset expansion interface provided with the E6xx processor. Instead, additional I/O can be attached to four ordinary PCI Express® lanes. The PC2-LIMBO is equipped with several PE based I/O controllers, e.g. SATA and Ethernet, and the EG20T PCH (Platform Controller Hub) for multi-function I/O.

As of current, the Atom™ E6xx family comprises processors from 0.6GHz up to 1.6GHz core frequency, either commercial or industrial temperature grade, as listed below. The processors are housed in a FCBGA package for direct soldering to the PCB, i.e. the chip cannot be removed or changed by the user.

Intel® Atom™ Processors Supported							
Processor Number	Core Clock	Gfx Clock	Operating Temperature	TDP	CPU ID	Stepping	SPEC Code
E620	*0.6GHz*	*320MHz*	*0°C to +70°C*	*3.3W*	*20661h*	*B1*	*SLJ32*
E640	*1.0GHz*	*320MHz*	*0°C to +70°C*	*3.6W*	*20661h*	*B1*	*SLJ33*
E660	*1.3GHz*	*400MHz*	*0°C to +70°C*	*3.6W*	*20661h*	*B1*	*SLJ34*
E680	1.6GHz	400MHz	0°C to +70°C	4.5W	20661h	B1	SLJ35
E620T	*0.6GHz*	*320MHz*	*-40°C to +85°C*	*3.3W*	*20661h*	*B1*	*SLJ36*
E640T	*1.0GHz*	*320MHz*	*-40°C to +85°C*	*3.6W*	*20661h*	*B1*	*SLJ37*
E660T	*1.3GHz*	*400MHz*	*-40°C to +85°C*	*3.6W*	*20661h*	*B1*	*SLJ38*
E680T	1.6GHz	400MHz	-40°C to +85°C	4.5W	20661h	B1	SLJ39

Thermal Considerations

The PC2-LIMBO is equipped with a low profile passive heatsink for fan-less conductive cooling, thus maintaining the 4HP envelope of a typical CompactPCI® card. In many situations a forced vertical airflow through the system enclosure (e.g. bottom mount fan unit) may be not required, due to the low power consumption of the Atom™ E6xx series, but should be considered to further improve the reliability and life-time of the assembly unit, especially for higher ambient temperatures.

The table above (Intel® Atom™ Processors Supported) indicates the calculated maximum power consumption (TDP = Thermal Design Power) of a particular processor. According to experience, the CPU power consumption is significantly lower when executing typical Windows® or Linux tasks.

The Atom™ E6xx processors provide thermal based Enhanced SpeedStep® technology. This enables dynamic switching between multiple core voltages and frequencies depending on core temperature and currently required performance. The processors are able to reduce their core speed and core voltage in multiple steps. This leads to an additional reduction of power consumption, resulting in less heating. This mode of lowering the processor core temperature is called Thermal Monitor 2.

Another way to reduce power consumption is to modulate the processor clock (Thermal Monitor 1 mode). When this feature is enabled and the die temperature is reaching the pre-determined activation temperature, the processor clocks are stopped for a period of time and then allowed to run full speed for a period of time (duty cycle ~30% – 50%) until the processor temperature drops below the activation temperature. However, while saving considerable power consumption, the data throughput of the processor is also reduced.

The temperature at which the on-die thermal sensor triggers the Intel® Thermal Monitor 1 or Intel® Thermal Monitor 2 is set during the fabrication of the processor (can be read-out by software).

The thermal management features are enabled under BIOS control (please observe related BIOS menu entries). By default the BIOS of the PC2-LIMBO enables the Thermal Monitor 2 mode which is the most efficient.

PC2-LIMBO with Custom Specific Cooler Plate

Main Memory

The Atom™ E6xx processor is equipped with an internal memory controller, suitable for a maximum capacity of 2GB DDR2, operated at 800MHz. The memory controller supports only soldered-down DRAM (no SODIMM).

The PC2-LIMBO is provided with either 1GB or 2GB memory, organized as 8 devices 1Gbit or 2Gbit each, soldered directly to the board (Memory Down). Please consider your actual need for a sufficient memory capacity before ordering.

Graphics Subsystem

The Intel® Atom™ Processor E6xx series provides an integrated 2D/3D graphic engine that performs pixel shading and vertex shading within a single hardware accelerator. The processing of pixels is deferred until they are determined to be visible, which minimizes access to memory and improves render performance. In addition, the E6xx series supports video decoding (MPEG2, MPEG4, VC1, WMV9, H.264, and DivX), and also encoding (MPEG4, H.264).

The PC2-LIMBO is provided with a DVI-D (digital video interface) front panel connector attached to the E6xx SDVO port via a PanelLink transmitter, for a maximum resolution up to 1920x1080.

Known issues: As of current, Intel® Embedded Graphics Drivers for the Atom™ Processor E6xx series must be used together with Windows 7. Ubuntu may not work as expected with respect to the graphics interface. Video decoding with Linux may be slow.

LAN Subsystem

The Ethernet LAN subsystem provided on the PC2-LIMBO is comprised of two independent Gigabit Ethernet ports. Both Ethernet ports are wired to correspondent RJ45 jacks located in the front panel, but can be also managed for usage through the rear I/O interface on J2/P2, on an individual base by BIOS settings. Two bicoloured LEDs integrated into each RJ45 connector in the front panel are used to signal the LAN link, the LAN connection speed and LAN activity status of the related Ethernet port, regardless whether it is routed to the front panel jack or to the backplane connector J2 for rear I/O.

There are two different Ethernet controllers populated on the PC2-LIMBO board; while port 1 is associated with the Platform Controller Hub, port 2 is realized with additional PCI Express® based silicon. This is the reason why both Ethernet ports offer slightly differing features.

The Platform Controller Hub EG20T (PCH, formerly named Topcliff IOH) contains a Gigabit Ethernet Media Access Controller (GMAC), which is connected to an external RGMII PHY (Reduced Gigabit Media Independent Interface) for 1000 BASE Ethernet. The PC2-LIMBO employs the Marvell 88E1116R Gigabit Ethernet Transceiver, which in turn is wired across a signal switch (under BIOS control) either to the upper RJ45 front panel Ethernet jack, or to J2 according to the CPCI 2.30 PlusIO standard. The maximum Jumbo frame size of the PCH EG20T is 10kB.

For the second Ethernet port the Intel® 82574IT GbE controller was chosen, which provides an integrated PHY and many built-in high performance features such as 802.1as TimeSync. It is wired across a signal switch (under BIOS control) either to the lower RJ45 front panel Ethernet jack, or to J2 according to the CPCI 2.30 PlusIO standard. The maximum Jumbo frame size of the 82574 is 9kB.

Serial ATA Interface (SATA)

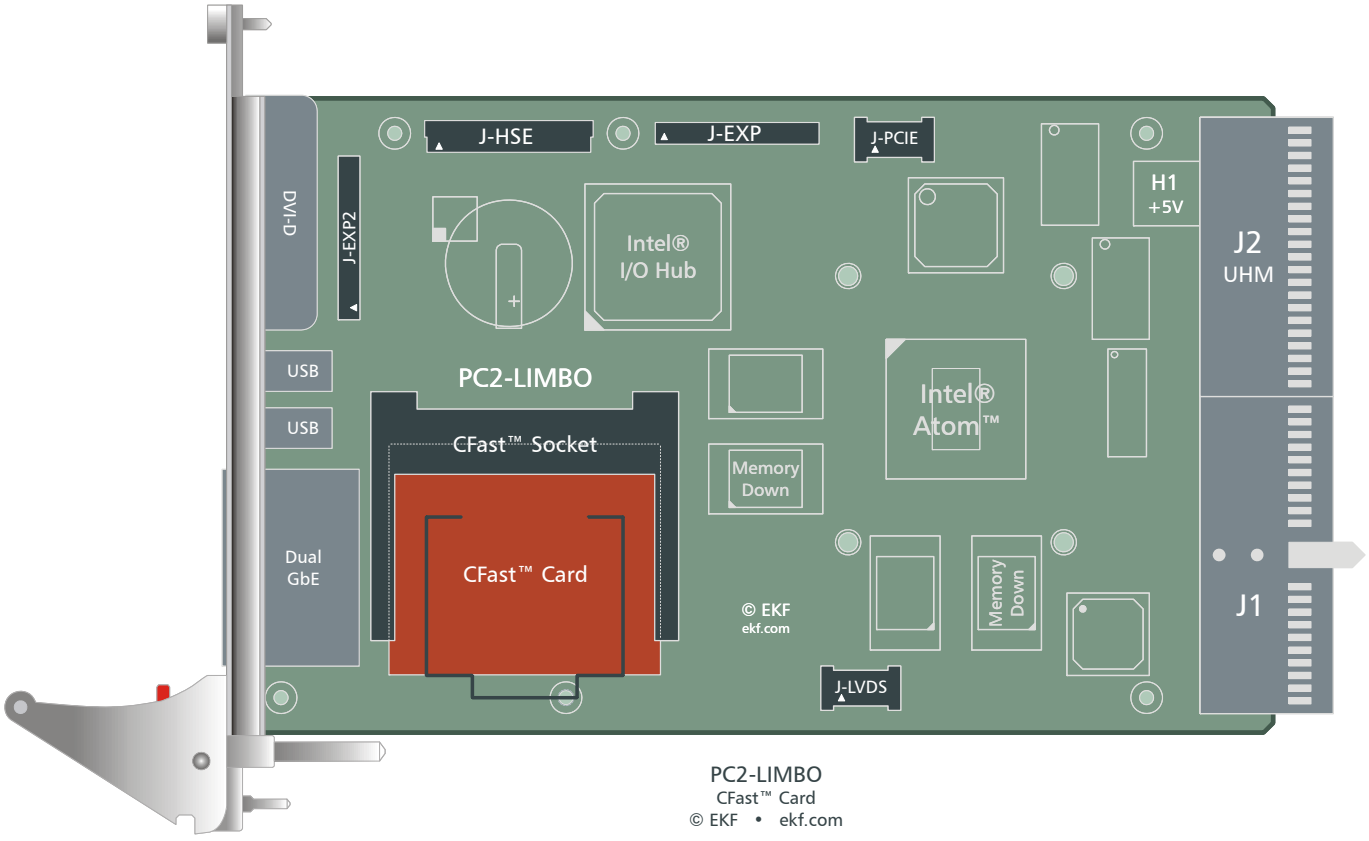
The PC2-LIMBO provides up to six 3Gbps serial ATA (SATA) ports, derived from three independent SATA ressources.

The EG20T Platform Controller Hub (PCH) is provided with an integrated SATA two-port controller. One of these ports is in use for the CFast™ host connector, the other is routed to first SATA port of the mezzanine card connector J-HSE (High Speed Expansion). Only these two SATA channels are suitable for attachment of a SATA boot medium.

Another two PCI Express® based SATA controllers (JMB362, dual-channel each) are populated in addition on the PC2-LIMBO. By default these channels are connected for rear I/O usage to the J2 PlusIO backplane connector, resulting in a maximum of 4 SATA channels for backplane usage (e.g. hybrid backplane in a CompactPCI® Serial system). As an ordering option, two SATA ports can be wired instead to the mezzanine connector J-HSE, as the 2nd and 3rd SATA port, which allows use of the C47-MSATA mezzanine storage module. As of current, the BIOS does not contain boot code for these dedicated SATA controllers. SATA boot therefore is possible either from the Cfast™ card, or from mezzanine storage modules such as the C42-SATA, which use the PCH bound 1st SATA channel of the J-HSE connector. The additional SATA controllers are not available with the CompactPCI® Classic manufacturing option of the PC2-LIMBO.

A LED named HD located in the front panel, signals disk activity status of any of the SATA devices.

The CFast™ host connector accommodates a modern Flash based Solid State Drive (SSD), with dimensions of a CompactFlash card, but SATA based interface. CFast™ cards are available from several manufacturers for the extended (industrial) temperature range, and can also be considered as boot device and system drive in small ruggedized systems.

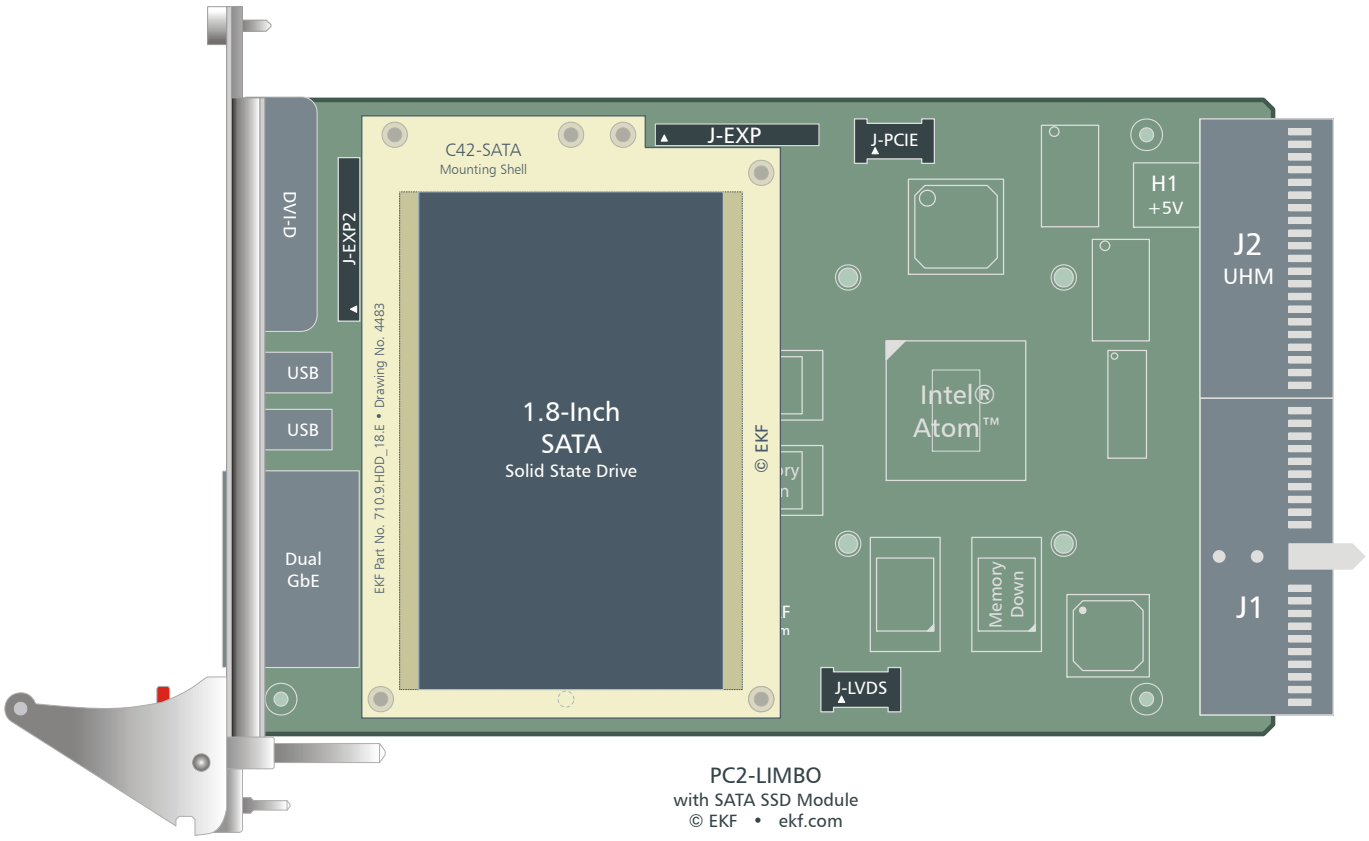


PC2-LIMBO
CFast™ Card
© EKF • ekf.com

As an option, the PC2-LIMBO can be equipped with a low profile mezzanine storage card such as the C42-SATA in addition, with an on-board 1.8-inch Micro SATA SSD, or the C47-MSATA, with two mSATA SSD modules. As of current, both mezzanine alternates offer higher storage capacity compared to a CFast™ card. A low profile mezzanine card can be used with or w/o simultaneously utilizing the CFast™ on-board card, and maintains the 4HP profile of the PC2-LIMBO.

Further more, a variety of side cards is available, suitable for mounting on the PC2-LIMBO in a 4HP (20.32mm) distance (resulting n 8HP front panel width for the assembly). Some of these side boards can accommodate a SATA drive, e.g. a 2.5-inch SSD. If more than one SATA channel is required for a side card with respect to the J-HSE mezzanine connector, the PC2-LIMBO must not be ordered with 4 SATA channels for backplane usage.

In addition to the EG20T PCH with its two SATA ports, two JMicron JMB362 dual-channel SATA controllers are stuffed on the PC2-LIMBO. Depending on the SATA channel in use, either Intel® SATA drivers for the EG20T have to be installed, and/or SATA drivers from the JMicron website.



PC2-LIMBO
with SATA SSD Module
© EKF • ekf.com

PCI Express® Interface

The Atom™ E6xx processor is provided with 4 x 1 PCI Express® (aka PCIe or PE) lanes for I/O expansion. Since this would be insufficient for a CPCI CPU card, the PC2-LIMBO is equipped with an 8-port PE packet switch in addition, for an adequate quantity of PCI Express® lanes available:

- 1 lane (CPU) connected to the Intel® EG20T Topcliff PCH
- 1 lane (CPU) connected to the PLX PE to PCI bridge (J1 CompactPCI® Classic backplane connector)
- 1 lane (CPU) connected to the Intel® 82574IT GbE controller
- 1 lane (CPU) connected to the 1:7 PE packet switch PLX PEX8608 (not populated together with the CPCI Classic Version of the PC2-LIMBO)

- 4 lanes (switch) available on the J2 rear I/O connector (e.g. for hybrid CompactPCI® Serial systems)
- 1 lane (switch) available on the mezzanine expansion card connector J-PCIE (derived directly from the PCH on the CPCI Classic Version of the PC2-LIMBO)
- 2 lanes (switch) required for the 2 x JMB362 on-board SATA controllers

Please note, that the CompactPCI® Classic version of the PC2-LIMBO does not provide the PCIe packet switch, and consequently will not be equipped with the JMB362 SATA controllers.

Universal Serial Bus (USB)

The EG20T (Topcliff) PCH supports a maximum of six USB 2.0 host ports. Since this would be insufficient for a CompactPCI® CPU card, the PC2-LIMBO is equipped with two on-board 1:4 USB hubs in addition, for an adequate quantity of USB ports available:

- 2 ports (PCH) connected to front panel USB receptacles
- 2 ports (PCH) connected to the mezzanine card legacy expansion connector J-EXP
- 1 port (PCH) connected to an USB hub (J2 usage)
- 1 port (PCH) connected to an USB hub (J-HSE usage)

- 4 ports (hub) connected to the rear I/O backplane connector J2
- 4 ports (hub) connected to the mezzanine card high speed expansion connector J-HSE

The PCH incorporates 6 OHCI controllers, and 2 EHCI controllers, for low, full and high speed operation.

Utility Interfaces

Besides the high speed mezzanine interface connectors J-HSE and J-PCIE, the PC2-LIMBO is provided with the utility interface expansion connector sockets J-EXP(1) and J-EXP2. These connectors comprise several interfaces, which may be useful for system expansion on a mezzanine card, as an option:

- CAN
- I^2C
- HD Audio
- LPC (Low Pin Count)
- PS/2 KBD/MS
- SDIO (SDHC Card)
- SMBus
- 2 x UART
- 2 x USB

The SMbus is controlled by the E6xx Tunnel Creek processor. The SMbus signal lines on the J-EXP utility expansion connector are buffered and can be switched on/off under software control (CPU GPIO) in order to isolate external components in case of an I^2C address conflict. *Please note: As of current, the SMbus has been permanently disabled*.

Another I^2C controller is integrated into the EG20T Topcliff PCH and wired to J-EXP2.

The HD Audio port requires an additional audio codec, as provided e.g. on the CCO-CONCERT side card. The UART channels are TTL level based and thus suitable for wiring to either EIA-232 or EIA-485 transceivers on the mezzanine card. The CAN port needs an external ISO transceiver for compliance.

EKF offers a variety of mezzanine expansion boards (side cards), to be attached on top of the PC2-LIMBO, thus typically resulting in a assembly unit with 8HP or even 12HP common front panel. Custom specific mezzanine cards can be designed to your needs - please contact sales@ekf.com.

Real-Time Clock

The Atom™ E6xx processor is equipped with a time-of-day clock and calendar. Battery backup is provided by a BR2032 Lithium Carbon monofluoride coin cell. The battery is suitable for the extended operating temperature range (-40°C to +85°C). Under *normal conditions*[1], replacement of the battery should be superfluous during lifetime of the board. In applications were the use of a battery is not permitted, a SuperCap (double layer capacitor, gold cap) with 1.0F capacity can be stuffed instead of the battery, sufficient for ~6h data retention.

[1] *Due to a known issue of the E6xx processor, the BR2032 battery lifetime may be significantly reduced, down to ~1 year as a worst case scenario. As of current Intel® classifies the status of this erratum as 'no fix'. Since the battery will be discharged only when power is disconnected from the CPU card, lifetime in typical industrial applications may not be affected (24h continuous-running operation in mind).*

SPI Flash

The BIOS is stored in flash device with Serial Peripheral Interface (SPI). 8MByte of BIOS code and user data may be stored nonvolatile in this SPI Flash.

The SPI Flash contents can be updated by a DOS or Linux based tool. This program and the latest PC2-LIMBO BIOS binary are available from the EKF website. Read carefully the enclosed instructions. If the programming procedure fails e.g. caused by a power interruption, the PC2-LIMBO may no more be operable. In this case you would possibly have to send in the board, because the Flash device is directly soldered to the PCB and cannot be changed by the user.

Reset

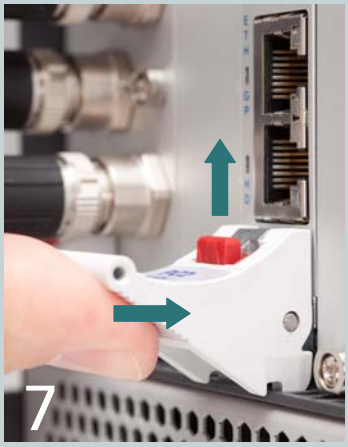
The PC2-LIMBO is provided with several supervisor circuits to monitor supply rails like the CPU core voltage, 1.5V, 3.3V or 5V. This circuitry is responsible also to generate a clean power-on reset signal.

The handle within the front panel contains a micro switch that is used to generate a power button event. By pressing the handle's red push button a pulse is triggered.
Animated GIF: www.ekf.com/c/ccpu/img/reset_400.gif

NOTE: To prevent the board to cause a power button override, the handle should be closed immediately after unlocking the front panel handle. A power button override is triggered by opening the front panel handle for at least 4 seconds, which results in bringing the board to power state S5. In case of entering this state, unlock and lock the front panel handle a 2nd time to reenter normal power state S0 again. See also section 'PG (Power Good) LED' to see how the PC2-LIMBO indicates the different power states.

An alternative (and recommended) way to generate a system reset is to activate the signal PRST# located on CompactPCI connector J2 pin C17. Pulling this signal to GND will have the same effect as to push a reset switch.

The healthy state of the PC2-LIMBO is indicated by the LED PG (Power Good) located in the front panel. This bicoloured LED signals different states of the board (see section below). As soon as this LED begins to lite green, all power voltages are within their specifications and the reset signal has been deasserted.



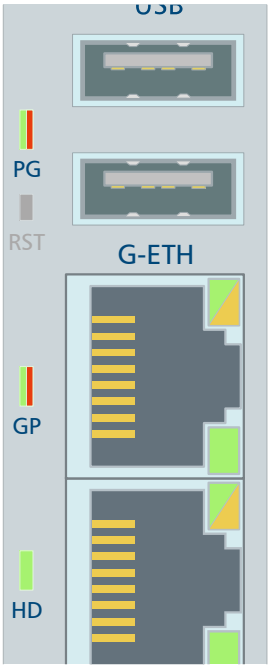
Watchdog

An important reliability feature is the watchdog function, which is programmable by software. The PC2-LIMBO is provided with a watchdog contained directly in the E6XX Tunnel Creek CPU. Another watchdog is available from the on-board SIO.

Front Panel LEDs

The PC2-LIMBO is equipped with three LEDs which can be observed from the front panel. These LEDs are labelled according to their primary meaning, but should be interpreted altogether for system diagnosis.

LED			Status
PG Green/Red	GP Green/Red	HD Green	
OFF	GREEN	ON	Sleep State S4/S5
OFF	OFF	ON	Sleep State S3
GREEN	RED BLINK	X	After Reset
GREEN	X	X	Board Healthy and in S0 State
GREEN	GREEN / GREEN BLINK	X	GP LED under Software Control (IOH GPIO5)
GREEN	X	ON / BLINK	SATA Activity
RED	X	X	Hardware Failure - Power Fault
RED BLINK	X	X	Software Failure



PG (Power Good) LED

The PC2-LIMBO offers a bicolour LED labelled PG located within the front panel. After system reset, this LED defaults to signal different power states:

- Off — Sleep state S3, S4 or S5 (S3/S4 deactivated by BIOS as of current, S5 = Soft Off)
- Green — Healthy
- Red steady — Hardware failure
- Red blink — Software failure

To enter the PG LED state *Software Failure,* an appropriate service request by software SMI must be called. The PG LED remains in this red blinking state until the next SMI request is made. After that it falls back to its default function.

GP (General Purpose) LED

This programmable bicolour LED can be observed from the PC2-LIMBO front panel. Its status is controlled by the on-board glue-logic (ispMACH 4128). The GP LED is not dedicated to any particular hardware or firmware function with exception of special power states of the LED PG as described above. Nevertheless, a red blinking GP LED is an indication that the BIOS code couldn't start.

The GP LED is provided mainly for user programming, e.g. can reflect the status of dedicated GPIOs under user software control, or any combination of other board internal signals available at the ispMACH programmable logic inputs. Please contact EKF in order to discuss your requirements in detail.

While the CPU card is controlled by the BIOS firmware, the GP LED is used to signal board status information. For details please refer to www.ekf.com/p/pc2/firmware/biosinfo.txt. After successful operating system boot, the GP LED may be freely used by customer software.

HD (Hard Disk Activity) LED

The PC2-LIMBO offers a green LED marked as HD placed within the front panel. This LED signals activity on any device attached to the SATA ports. This includes the EG20T IOH SATA ports as well as the JMicron SATA controllers.

The marking HD denotes a hard disk drive, but needless to say that also activity from solid state drives (SSD) such as a CFast card would light the HD LED. As previously described, this LED may vary its function dependent on the state of the LED PG.

Hot Swap Detection

The CompactPCI® specification added the signal ENUM# to the PCI bus to allow board hot swapping. This signal is routed to a GPIO (GPIO1 PEX8112 PCIe to PCI bridge) . An interrupt can be requested, if ENUM# changes, caused by insertion or removal of a peripheral board.

Note that the PC2-LIMBO itself is not a hot swap device, because it makes no sense to remove the system controller from a CompactPCI® system. However, it is capable to recognize the hot swap of peripheral boards and to start software that is performing any necessary system reconfiguration.

Power Supply Status (DEG#, FAL#)

Power supply failures may be detected before the system crashes down by monitoring the signals DEG# or FAL#. These active low lines are additions to the CompactPCI® specification and may be driven by the power supply. DEG# signals the degrading of the supply voltages, FAL# there possible failure. On the PC2-LIMBO the signals FAL# and DEG# are routed to PCH GPIOS.

+5V Only Design

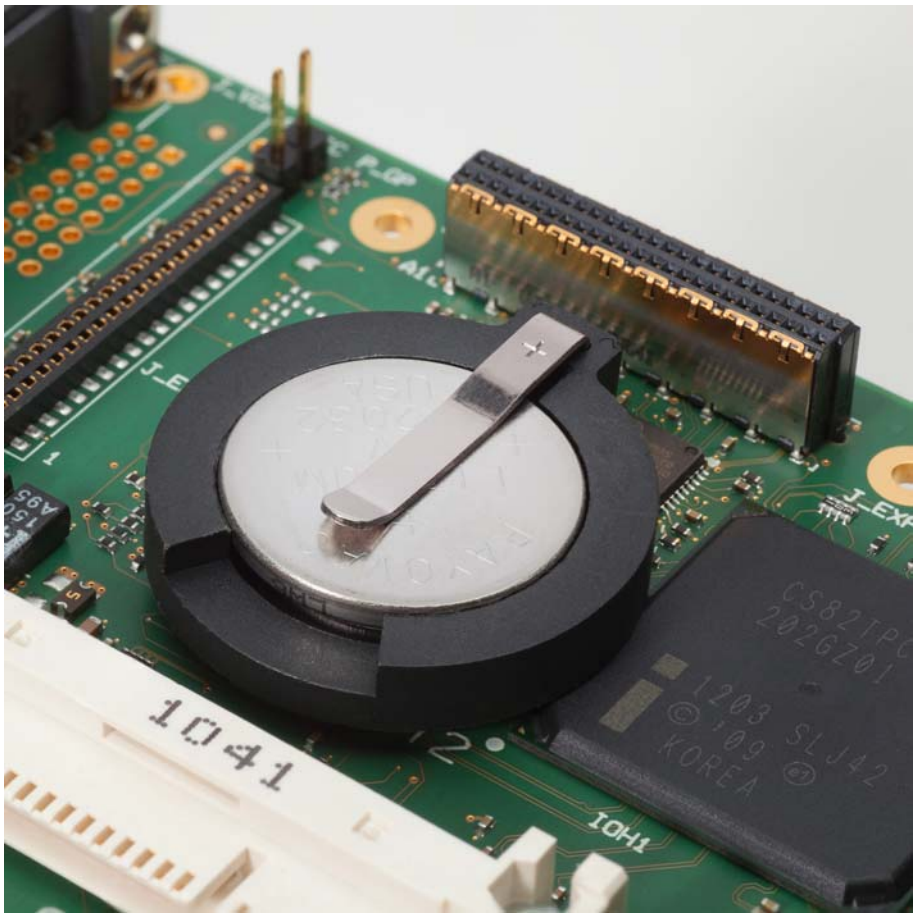
The PC2-LIMBO has been designed for +5V only operation. For system cost reduction, the on-board switching regulator from +5V to +3.3V can be used to feed-back +3.3V through connector J1 to the CompactPCI® backplane in systems with a single +5V power supply.

The on-board 3.3V switching regulator has been designed for a maximum of 10A load in total. Since the +3.3V rail is shared with on-board components and optional mezzanine cards, the maximum current available for peripheral boards on the CompactPCI® backplane depends on the actual configuration of the PC2-LIMBO. Typically, the PC2-LIMBO would be able to source up to 5A into the backplane +3.3V power rail. This would require a soldered 15A fuse to be populated as an option, placed in series between the on-board +3.3V rail and the backplane connector J1 3.3V pins.

By default, the soldered 15A fuse is not populated. For systems with a dual-rail power supply which provides +3.3V to the CPCI backplane, the fuse should be removed (if populated), in order to avoid a current back-driving situation. Under normal conditions, back-driving +3.3V power from the backplane to the board and vice versa should be permissible, but EKF cannot guarantee this, due to numerous available system power supplies with different characteristics.

Battery Options

By default, the PC2-LIMBO is equipped with a battery holder, which is suitable for a BR2032 coin type Lithium cell. For rugged applications, a soldered cell may be populated. A third stuffing alternate would be a gold cap.



Coin Cell Holder (Default Stuffing)

Please remove the isolating plastic sheet from the coin cell which may be affixed in order to avoid premature discharge of the battery.

Unfortunately, Intel® describes a severe issue with the battery, which is not expected to be fixed with future versions of the Tunnelcreek processor. There exists a leakage path, which may reduce the typical lifetime of a cell to <1year, when the PC2-LIMBO is not powered (during storage, or when the system is shut down).

The 1.0F rechargable double layer capacitor can be populated as an alternate for such applications, where a battery would not be allowed. Data retention however would be limited to <8h typically. Low profile C4* mezzanine modules cannot be used when the supercap is stuffed due to its height.

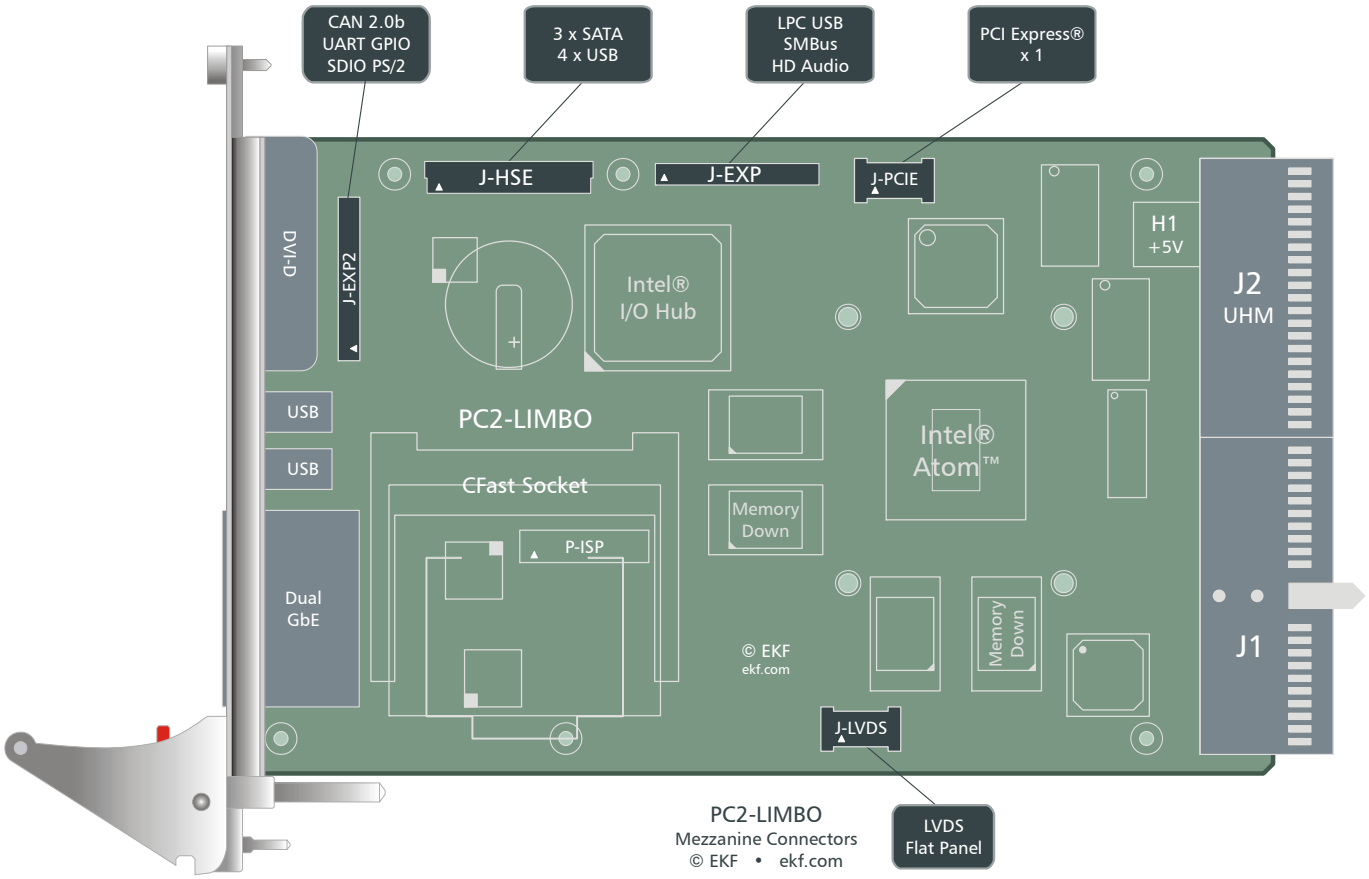
Due to a known issue of the E6xx processor, the BR2032 battery lifetime may be significantly reduced, down to ~1 year as a worst case scenario. As of current Intel® classifies the status of this erratum as 'no fix'. Since the battery will be discharged only when power is disconnected from the CPU card, lifetime in typical industrial applications may not be affected (24h continuous-running operation in mind).

Option Soldered Lithium Cell

Option Supercapacitor

Mezzanine Side Board Options

The PC2-LIMBO is provided with several stacking connectors for attachment of a mezzanine expansion module (aka side board), suitable for a variety of readily available mezzanine cards (please refer to www.ekf.com/c/ccpu/mezz_ovw.pdf for a more comprehensive overview). EKF furthermore offers custom specific development of side boads (please contact sales@ekf.de).



Most mezzanine expansion modules require an assembly height of 8HP in total, together with the CPU carrier board (resulting from two cards at 4HP pitch each).

In addition, cropped low profile mass storage mezzanine modules can be attached to J-HSE, which maintain the 4HP envelope, for extremely compact systems. Furthermore these small size modules may be combined with the full-size expansion boards (that means an assembly comprised of 3 PCBs).

Related Documents Mezzanine Modules and Side Cards	
C4x Series Mezzanine Storage Modules	www.ekf.com/c/ccpu/c4x_mezz_ovw.pdf
Mezzanine Modules Overview	www.ekf.com/c/ccpu/mezz_ovw.pdf
The EKF Mezzanine Module Concept	www.ekf.com/c/ccpu/cpci_mezzanine_evolution.pdf

J-EXP(1)	
I/F Type	Controller
LPC (Low Pin Count)	CPU
HD Audio	CPU
SMBus	CPU (buffered)
2 x USB 2.0	PCH

J-EXP2 (not poulated by default)	
I/F Type	Controller
CAN	PCH
I^2C	PCH
PS/2 KBD/MS	SIO
SDIO (SDHC Card)	PCH
2 x UART	PCH

J-HSE	
I/F Type	Controller
SATA1	PCH
SATA2, SATA3	JMB362 (option only, on request)
4 x USB 2.0	USB Hub

J-LVDS (not poulated by default)	
I/F Type	Controller
LVDS Video	CPU

J-PCIE	
I/F Type	Controller
PCI Express®	PE Switch (CompactPCI® PlusIO) PCH (CompactPCI® Classic version)

PC2-LIMBO (Top View)

CompactPCI® PlusIO Option

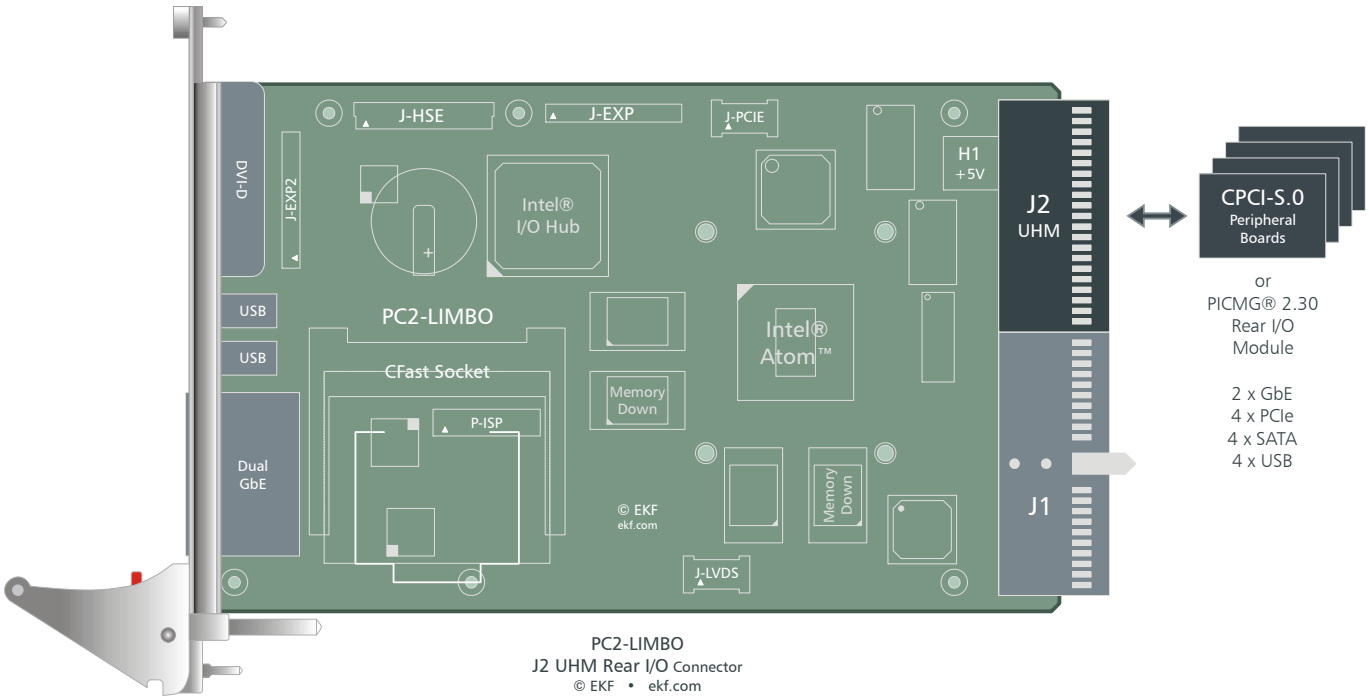
The PICMG® 2.30 CompactPCI® PlusIO specification defines the usage of rear I/O pins of the 32-bit CompactPCI® system slot for high-speed serial signals. For these high-speed signals a new J2 connector (3M UHM type) has been introduced, which is compatible to the classic 2.0mm hard metric connector J2, and in addition is suitable for high speed differential signals.

The main advantage of the combination of legacy PCI (J1/P1) and modern serial buses on J2/P2 is to realize hybrid backplanes. Hence, the CompactPCI® PlusIO standard helps to define a simple migration path from parallel PCI systems to modern serial, point-to-point interconnected systems such as CompactPCI® Serial (PICMG® CPCI-S.0, draft/proposal as of current).

PICMG® 2.30 defines just the system slot J2/P2 extension. With respect to high speed signal peripheral boards – depending on their particular interfaces – CompactPCI® Serial, CompactPCI® Express or PICMG® 2.16 cards may be combined in a system, in addition to 32-bit classic CompactPCI® boards, controlled across J1/P1.

The PC2-LIMBO is provided with all CompactPCI® PlusIO communication channels defined by PICMG® 2.30 via the connector J2/P2:

- Four PCIe Lanes 2.5GT/s
- Up to four SATA Ports 3GT/s
- Four USB 2.0 Ports
- Up two Gigabit Ethernet Ports



J2 UHM Connector According to PICMG 2.30 PlusIO

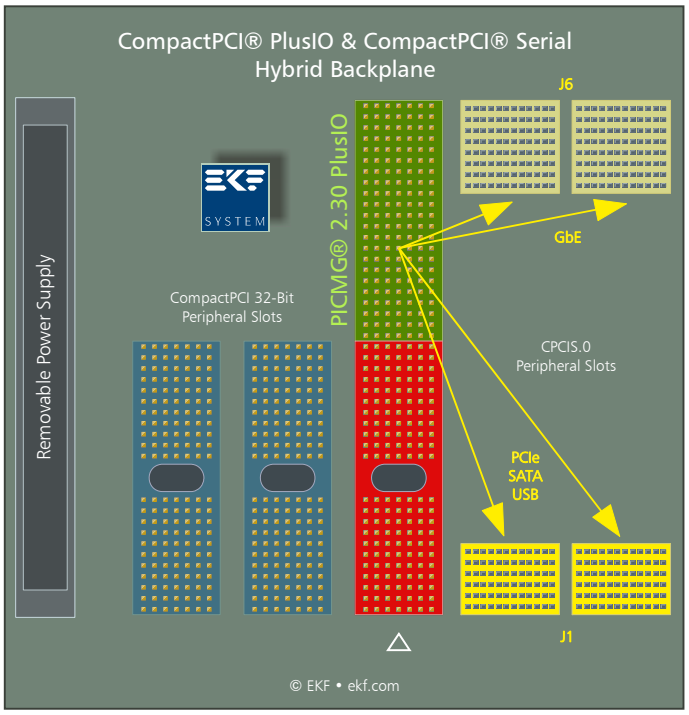
Warning: Do not operate the PC2-LIMBO in systems with a 64-bit CompactPCI® backplane. The J2/P2 pin assignments of a 64-bit CPCI backplane differ substantially from a CompactPCI® PlusIO backplane, which may result in a short circuit situation.

The PC2-LIMBO can be combined with a CompactPCI® PlusIO rear I/O transition module, such as the PR1-RIO, which is provided with I/O connectors (on-board and back-panel) for all high speed signals.

Sample PlusIO RIO Module

Related Documents CompactPCI® PlusIO & CompactPCI® Serial	
CompactPCI® PlusIO & Serial Overview	www.ekf.com/s/cpci_serial_overview.pdf
CompactPCI® PlusIO Home	www.ekf.com/p/plus.html
CompactPCI® Serial Home	www.ekf.com/s/serial.html

Hybrid systems can be configured by means of a backplane with CompactPCI® Serial slots in addition to classic CompactPCI® slots.



Sample Hybrid Backplane

Sample Hybrid Backplane

The PC2-LIMBO can be used as a system controller for a CompactPCI® Serial system, by means of a suitable hybrid backplane.

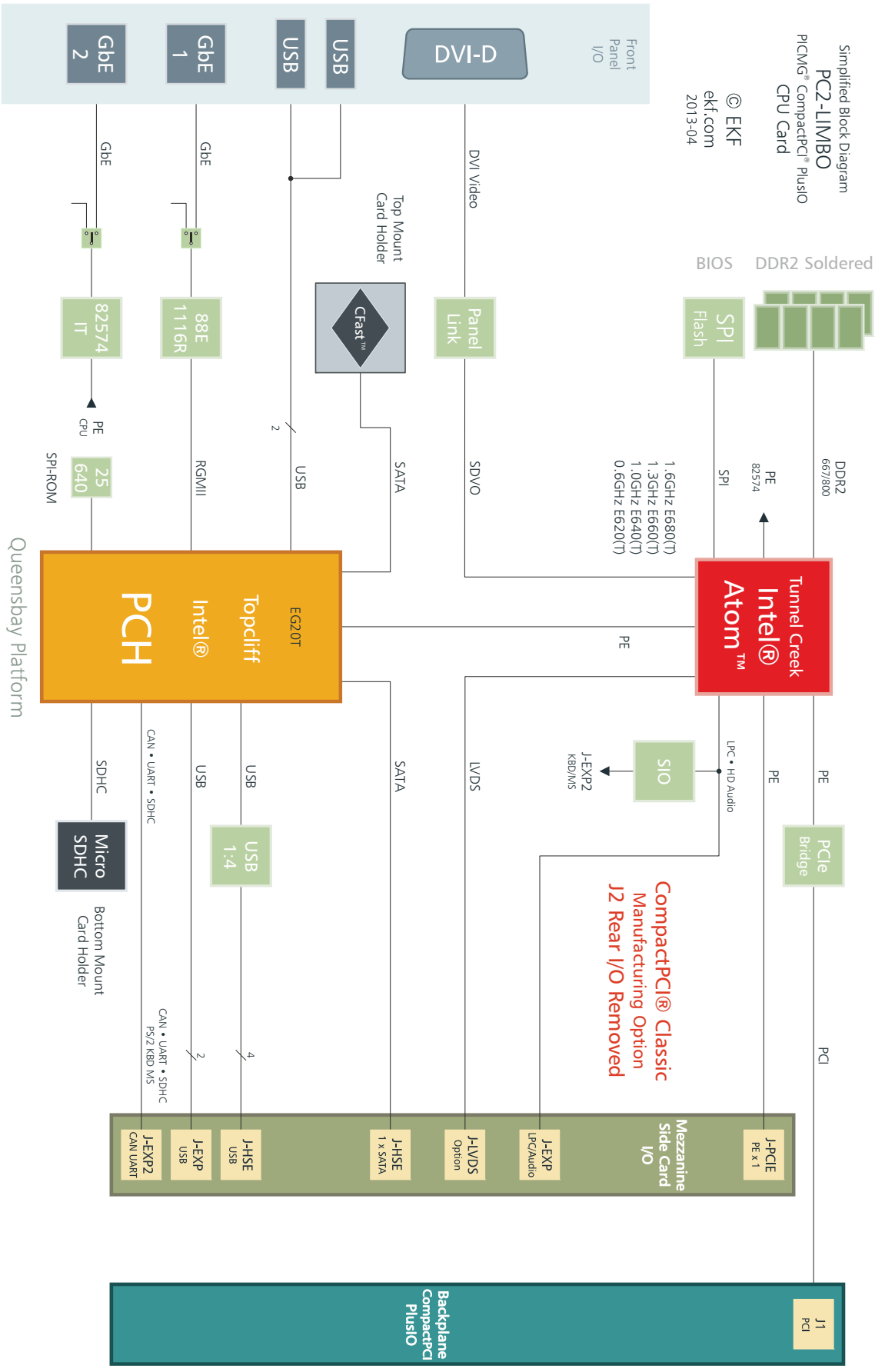
Rugged Industrial Systems

Rugged Industrial Systems

CompactPCI® Classic Option

As a PC2-LIMBO manufacturing option, all J2 rear I/O connections according to the PICMG® 2.30 CompactPCI® PlusIO specification can be removed, by not filling related components (e.g. PCIe switch, USB hub, Ethernet magnetics). This option is useful for systems equipped with a 32-bit legacy 2.0 CompactPCI® backplane. Please refer to www.ekf.com/liste/liste_21.html#PC2 for manufacturing option SKUs available.

Please note, that open PCB copper traces to J2 are still existent, which may downgrade the P2 backplane signal quality (stubs).



Block Diagram PC2-LIMBO CompactPCI 2.0 Option

Installing and Replacing Components

Before You Begin

Warnings

The procedures in this chapter assume familiarity with the general terminology associated with industrial electronics and with safety practices and regulatory compliance required for using and modifying electronic equipment. Disconnect the system from its power source and from any telecommunication links, networks or modems before performing any of the procedures described in this chapter. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage. Some parts of the system can continue to operate even though the power switch is in its off state.

Caution

Electrostatic discharge (ESD) can damage components. Perform the procedures described in this chapter only at an ESD workstation. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis or board front panel. Store the board only in its original ESD protected packaging. Retain the original packaging (antistatic bag and antistatic box) in case of returning the board to EKF for rapair.

Installing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system 
- Remove the board packaging, be sure to touch the board only at the front panel
- Identify the related *CompactPCI* slot (peripheral slot for I/O boards, system slot for CPU boards, with the system slot typically most right or most left to the backplane)
- Insert card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- A card with onboard connectors requires attachment of associated cabling now
- Lock the ejector lever, fix screws at the front panel (top/bottom)
- Retain original packaging in case of return

Removing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system
- Identify the board, be sure to touch the board only at the front panel
- unfasten both front panel screws (top/bottom), unlock the ejector lever
- Remove any onboard cabling assembly
- Activate the ejector lever
- Remove the card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- Store board in the original packaging, do not touch any components, hold the board at the front panel only

Warning

Do not expose the card to fire. Battery cells and other components could explode and cause personal injury.

EMC Recommendations

In order to comply with the CE regulations for EMC, it is mandatory to observe the following rules:

- The chassis or rack including other boards in use must comply entirely with CE
- Close all board slots not in use with a blind front panel
- Front panels must be fastened by built-in screws
- Cover any unused front panel mounted connector with a shielding cap
- External communications cable assemblies must be shielded (shield connected only at one end of the cable)
- Use ferrite beads for cabling wherever appropriate
- Some connectors may require additional isolating parts

Reccomended Accessories

Blind CPCI Front Panels	EKF Elektronik	Widths currently available (1HP=5.08mm): with handle 4HP/8HP without handle 2HP/4HP/8HP/10HP/12HP
Ferrit Bead Filters	ARP Datacom, 63115 Dietzenbach	Ordering No. 102 820 (cable diameter 6.5mm) 102 821 (cable diameter 10.0mm) 102 822 (cable diameter 13.0mm)
Metal Shielding Caps	Conec-Polytronic, 59557 Lippstadt	Ordering No. CDFA 09 165 X 13129 X (DB9) CDSFA 15 165 X 12979 X (DB15) CDSFA 25 165 X 12989 X (DB25)

Replacement of the Battery

When your system is turned off, a battery maintains the voltage to run the time-of-day clock and to keep the values in the CMOS RAM. The battery should last during the lifetime of the PC2-LIMBO (please note a known E6XX CPU chip issue which is not fixed as of current). For replacement of a soldered Lithium cell, the old battery must be desoldered, and the new one soldered. We suggest that you send back the board to EKF for soldered battery replacement.

Coin Cell Holder (Default Stuffing)

Option Soldered Lithium Cell

Warning

Danger of explosion if the battery is incorrectly replaced or shorted. Replace only with the same or equivalent type. Do not expose a battery to fire.

Technical Reference

Local PCI Devices

The following table shows the on-board PCI devices and their location within the PCI configuration space.

Bus #	Device #	Function #	Vendor ID	Device ID	Description
0	0	0	0x8086	0x4114	E6xx Host Bridge
0	1	0	0x8086	0x8183	E6xx Configuration Unit
0	2	0	0x8086	0x4108	E6xx Graphics Controller
0	3	0	0x8086	0x8182	E6xx Video Multimedia
0	17	0	0x8086	0x8184	E6xx PCIe Port 1
0	18	0	0x8086	0x8185	E6xx PCIe Port 2
0	19	0	0x8086	0x8180	E6xx PCIe Port 3
0	1A	0	0x8086	0x8181	E6xx PCIe Port 4
0	1F	0	0x8086	0x8186	E6xx LPC Bridge
01	00	0	0x8086	0x8800	EG20t PCIe Port
02	00	0	0x8086	0x8801	EG20T Packet Hub
02	00	1	0x8086	0x8802	EG20T Ethernet MAC
02	00	2	0x8086	0x8803	EG20T GPIO
02	02	0	0x8086	0x8804	EG20T USB Host1 OHCI 0
02	02	1	0x8086	0x8805	EG20T USB Host1 OHCI 1
02	02	2	0x8086	0x8806	EG20T USB Host1 OHCI 2
02	02	3	0x8086	0x8807	EG20T USB Host1 EHCI
02	02	4	0x8086	0x8808	EG20T USB Device (Client)
02	04	0	0x8086	0x8809	EG20T SDIO Controller 1
02	04	1	0x8086	0x880A	EG20T SDIO Controller 2
02	06	0	0x8086	0x880B	EG20T SATA Controller
02	08	0	0x8086	0x880C	EG20T USB Host0 OHCI 0
02	08	1	0x8086	0x880D	EG20T USB Host0 OHCI 1
02	08	2	0x8086	0x880E	EG20T USB Host0 OHCI 2
02	08	3	0x8086	0x880F	EG20T USB Host0 EHCI
02	0A	0	0x8086	0x8810	EG20T DMA
02	0A	1	0x8086	0x8811	EG20T UART 0
02	0A	2	0x8086	0x8812	EG20T UART 1
02	0A	3	0x8086	0x8813	EG20T UART 2
02	0A	4	0x8086	0x8814	EG20T UART 3

Bus #	Device #	Function #	Vendor ID	Device ID	Description
02	0C	0	0x8086	0x8815	EG20T DMA
02	0C	1	0x8086	0x8816	EG20T SPI
02	0C	2	0x8086	0x8817	EG20T I2C
02	0C	3	0x8086	0x8818	EG20T CAN
02	0C	4	0x8086	0x8819	EG20T IEEE1588
03	00	0	0x8086	0x10D3	Ethernet Controller N2 (82574)
04	00	0	0x10B5	0x8608	PCIe Switch (PEX8608)
05	01	0	0x10B5	0x8608	PCIe Switch (PEX8608)
05	04	0	0x10B5	0x8608	PCIe Switch (PEX8608)
05	05	0	0x10B5	0x8608	PCIe Switch (PEX8608)
05	06	0	0x10B5	0x8608	PCIe Switch (PEX8608)
05	07	0	0x10B5	0x8608	PCIe Switch (PEX8608)
05	08	0	0x10B5	0x8608	PCIe Switch (PEX8608)
05	09	0	0x10B5	0x8608	PCIe Switch (PEX8608)
08	00	0	0x197B	0x2362	PCIe - SATA Controller (JMB 362)
0C	00	0	0x197B	0x2362	PCIe - SATA Controller (JMB 362)
0D	00	0	0x10B5	0x8112	PCIe to PCI Bridge (8112)

1) Depends on BIOS settings

2) Bus number can vary depending on the PCI enumeration schema implemented in BIOS

Local SMB Devices

The PC2-LIMBO contains devices that are attached to the System Management Bus (SMBus). These are the clock generation chip, the SPD EEPROMs for the on-board memory, a general purpose serial EEPROM and a supply voltage and temperature controlling device in particular. Additional devices may be connected to the SMBus via the CompactPCI backplane signals IPMB SCL (J1 B17) and IPMB SDA (J1 C17), or pins 29/30 of the mezzanine expansion connector J-EXP.

Address	Description
0x58	Hardware Monitor/CPU Temperature Sensor (LM87)
0xA0	SPD of Onboard Memory
0xAE	General Purpose EEPROM
0xD3	Power and Clock supply IC (DA6011)

Hardware Monitor LM87

Attached to the SMBus, the PC2-LIMBO is provided with a hardware monitor (LM87). This device is capable to observe the board and an the memory temperature, as well as several supply voltage rails with a resolution of 8 bit. The following table shows the mapping of the voltage inputs of the LM87 to the corresponding supply voltages of the PC2-LIMBO:

Input	Source	Resolution [mV]	Register
AIN1	E6xx Processor Core Voltage VCC	9.8	0x28
AIN2	E6xx Graphics Core Voltage VNN	9.8	0x29
VCCP1	+1.5V	14.1	0x21
VCCP2/D2-	+1.8V	14.1	0x25
+2.5V/D2+	+1.05V	13	0x20
+3.3V	+3.3V	17.2	0x22
+5V	+5V	26	0x23
+12V	GND	62.5	0x24

Beside the continuous measuring of temperatures and voltages the LM87 may compare these values against programmable upper and lower boundaries. As soon as a measurement violates the allowed value range, the LM87 can request an interrupt via the GPE# (General Purpose Event) input of the Tunnel Creek CPU (which may result in a system control interrupt).

GPIO Usage

GPIO Usage Tunnel Creek CPU

GPIO Usage Tunnel Creek CPU				
GPIO	Type	Tol.	Function	Description
GPIO_SUS0	I/O	3.3V	N/A	Not used on PC2
GPIO_SUS1	O	3.3V	BKLTEN	LVDS backlight enable (not implemented)
GPIO_SUS2	O	3.3V	BKLTCTL	LVDS backlight control (not implemented)
GPIO_SUS3	O	3.3V	VGA_DDCCL	LVDS DDC CLK (not implemented)
GPIO_SUS4	I/O	3.3V	VGA_DDCDA	LVDS DDC DATA (not implemented)
GPIO_SUS5	O	3.3V	NIC2_SWITCH	Switch Ethernet Controller NC2 to Front / Rear
GPIO_SUS6	O	3.3V	NIC1_SWITCH	Switch Ethernet Controller NC1 to Front / Rear
GPIO_SUS7	I	3.3V	EXP_SMI#	Expansion Interface SMI Request (J-EXP Pin15)
GPIO_SUS8	O	3.3V	NIC2_OFF#	Disable Ethernet Controller NC2
GPIO 0	I/O	3.3V	N/A	Not used on PC2 (pulled via resistor to 3.3V)
GPIO 1	I	3.3V	CPCI_INTP_33#	Compact PCI Interrupt Request Line INTP
GPIO 2	O	3.3V	J1_SMB_ISOLATE#	Isolate local SMBus of CPCI IPMB LOW: IPMB disconnected from SMBus HIGH: IPMB connected to SMBus
GPIO 3	O	3.3V	EXP_SMB_ISOLATE#	Isolate local SMBus of J-EXP LOW: J-EXP disconnected from SMBus HIGH: J-EXP connected to SMBus
GPIO 4	I/O	3.3V	N/A	Not used on PC2 (pulled via resistor to GND)

GPIO Usage Topcliff PCH

GPIO Usage Topcliff PCH					
GPIO	Type	Tol.	Function	Description	
GPIO 0		3.3V [1]	CPCI_DEG#	Compact PCI Power Degeneration Line DE#	
GPIO 1		3.3V [1]	CPCI_FAL#	Compact PCI Power Failure Line FAL#	
GPIO 2-4		3.3V [1]	HW_REV0...2	GPIO 4/3/2 000 001 ... 111	PCB Revision 0 1 ... 7
GPIO 5		3.3V [1]	IOH_GPLED	General Purpose LED Control (via PLD)	
GPIO 6		3.3V [1]	PLD_SDA	Local Option Reg Interface (within PLD)	
GPIO 7		3.3V [1]	PLD_SCL	Local Option Reg Interface (within PLD)	
GPIO 8		3.3V [2]	CPCI_INTSEN	Connect SERIRQ to Compact PCI Line INTS LOW: SERIRQ disconnected from INTS HIGH: SERIRQ connected to INTS	
GPIO 9		3.3V [2]	CPCI_SYSEN#	Sense Compact PCI System Slot Enable Line SYSEN#	
GPIO 10		3.3V [2]	GP_JUMPER	Reset UEFI BIOS Setup, Jumper P-GP	
GPIO 11		3.3V [2]	CPCI_CLKBUF_EN	Enables CPCI Clocks LOW: Compact PCI Clocks disabled HIGH: Compact PCI Clocks enabled	

[1] Active in S0 and S3, 5V tolerant.
[2] Active in S0 only.

GPIO Usage PE Switch

GPIO Usage PCI Express® Switch				
GPIO	Type	Tol.	Function	Description
GPIO 0	O	3.3V	CFAST_CDI	CFast Card detect input
GPIO 1	I	3.3V	CFAST_CDA	CFast Card detect output
GPIO 2-16	I/O	3.3V	N/A	Not used on PC2
GPIO 29	I/O	3.3V	N/A	Not used on PC2
GPIO 30	I/O	3.3V	N/A	Not used on PC2

GPIO Usage PE to PCI Bridge

GPIO Usage PEX8112				
GPIO	Type	Tol.	Function	Description
GPIO 0	I/O	3.3V	N/A	Not used on PC2 (pulled via resistor to 3.3V)
GPIO 1	I	3.3V	CPCI_ENUM_33#	Compact PCI System Enumeration Line ENUM#
GPIO 2	I/O	3.3V	N/A	Not used on PC2 (pulled via resistor to 3.3V)
GPIO 3	I/O	3.3V	N/A	Not used on PC2 (pulled via resistor to 3.3V)

Configuration Jumpers

CMOS Reset (P-GP)

The jumper P-GP may be used to reset the UEFI BIOS configuration to a default state. The UEFI BIOS on PC2-LIMBO stores parts of its configuration values in an area within the BIOS flash, e.g. the actual boot devices. Using this jumper is only necessary, if it is not possible to enter the setup of the BIOS. To reset the settings mount a jumper on P-GP and perform a system reset. As long as the jumper is stuffed the BIOS will use the default CMOS values after any system reset. To get normal operation again, the jumper has to be removed.

P-GP

P-GP	Function
Jumper Removed [1)]	normal operation
Jumper Installed	UEFI BIOS configuration reset to factory default

RTC Reset (P-RTC)

The jumper P-RTC may be used to reset certain register bits of the real time clock (part of the Tunnel Creek CPU). This can be necessary under rare conditions (e.g. battery undervoltage), if the CPU fails to enter the BIOS POST after power on. Note that installing of jumper P-RTC will neither perform the clearing of the CMOS RAM values nor resets the time and date register values of the real time clock. To reset the RTC core the board must be removed from the system rack. Short-circuit the pins of P-RTC for about 1 sec. Thereafter reinstall the board to the system and switch on the power. It is important to accomplish the RTC reset while the board has no power. The pin header P-RTC is not stuffed on the PC2-LIMBO by default.

P-RTC

P-RTC	Function
Jumper Removed [1)]	No RTC reset performed
Jumper Installed	RTC reset performed

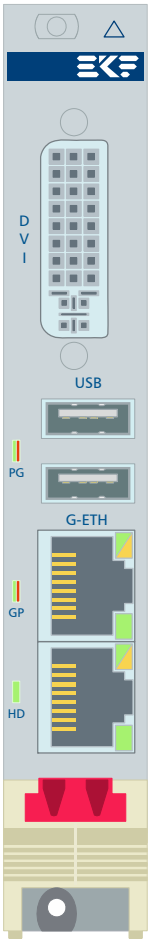
[1)] This setting is the factory default.

Connectors

Caution

Some of the internal connectors provide operating voltage (3.3V and 5V) to devices inside the system chassis, such as internal peripherals. Not all of these connectors are short circuit protected. Do not use these internal connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the board, the interconnecting cable and the external devices themselves.

Front Panel Connectors



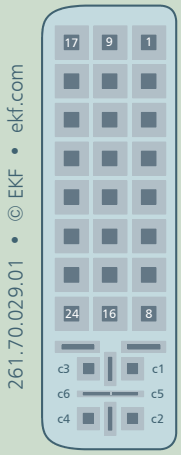
PC2-LIMBO

PC2-LIMBO (Front View)

DVI Video Connector

The Intel® Atom™ E6xx Tunnel Creek processor is equipped with an integrated graphics controller, which supports LVDS and SDVO display ports. On the PC2-LIMBO only the SDVO channel is used for video output. The LVDS port is wired to the optional mezzanine connector J-LVDS, for future use on custom specific side cards.

For compatibility with all types of DVI cables, the video front panel receptacle is a DVI-I style connector. However, the connector comprises the digital signals only, which results in DVI-D functionality. The digital video output is derived from the SDVO graphics port of the CPU, via a PanelLink transmitter.



DVI

DVI						
17	TX0-	9	TX1-	1	TX2-	
18	TX0+	10	TX1+	2	TX2+	
19	GND	11	GND	3	GND	
20		12		4		
21		13		5		
22	GND	14	DDC_POW [1)]	6	DDC_SCL	
23	TXC+	15	GND	7	DDC_SDA	
24	TXC-	16	DVI_HP	8	*VSYNC*	
	c3	*BLUE*	c1	*RED*		
	c6	GND	c5	GND		
	c4	*HSYNC*	c2	*GREEN*		

signals marked grey/italic: not supported

1) +5V via self resetting fuse 0.75A

Attachment of a single digital monitor (flat panel display) should be done by means of a DVI to DVI cable (DVI-D single link cable is sufficient).

For attachment of a single analog (VGA) monitor to the J-DVI receptacle, there are both adapters and also adapter cables available from DVI to the legacy HD-SUB15 VGA style connector.

USB Connectors

The Intel® EG20T (Topcliff) PCH (Platform Controller Hub) incorporates a six-port USB 2.0 host controller. Two ports are directly available on the PC2-LIMBO front panel (type A receptacle), for attachment of external USB devices.

USB Ports 1/2		
 #270.20.04.2 ©EKF • ekf.com	1	POW [1]
	2	USB DATA (N)
	3	USB DATA (P)
	4	GND

[1] +5V via 1.5A current-limited electronic power switch. Power rail may be switched off by software independently for each port.

Ethernet Connectors

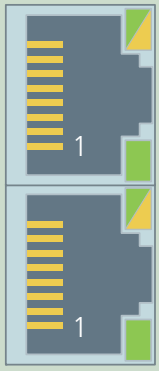
The PC2-LIMBO provides two independent Gigabit Ethernet controllers, each with its own MAC address.

The EG20T PCH contains an Ethernet MAC, which is complemented by an additional on-Board PHY, which is wired to the upper RJ-45 Ethernet jack 1 (if not redirected to the PlusIO J2 connector for RIO usage).

The second Ethernet controller is a 82574IT with integrated PHY, which is wired to the lower RJ-45 Ethernet jack 2 (if not redirected to the PlusIO J2 connector for RIO usage).

Both Ethernet ports are routed individually across two-way analog signal switches, for front panel usage, or optional redirection to the backplane connector J2 (for employment on a RIO module such as the PR1-RIO, or utilization on a CompactPCI® Serial backplane). While the front panel Ethernet jacks comprise internal magnetics, the PC2-LIMBO is equipped in addition with discrete magnetics modules for rear I/O.

The direction (front panel or RIO) of either Gigabit Ethernet port is controlled via two processor GPIO lines, which are managed by the BIOS: GPIO_SUS6 switches the Ethernet port 1, and GPIO_SUS5 controls port 2. The default routing is front panel usage. Please adjust the PC2-LIMBO BIOS settings for an alternate configuration.

Gigabit Ethernet Ports 1/2 (RJ-45)			
 270.02.08.5	Port 1	1	NC1_MDX0+
		2	NC1_MDX0-
		3	NC1_MDX1+
		4	NC1_MDX2+
		5	NC1_MDX2-
		6	NC1_MDX1-
		7	NC1_MDX3+
		8	NC1_MDX3-
	Port 2	1	NC2_MDX0+
		2	NC2_MDX0-
		3	NC2_MDX1+
		4	NC2_MDX2+
		5	NC2_MDX2-
		6	NC2_MDX1-
		7	NC2_MDX3+
		8	NC2_MDX3-

The lower green LED indicates LINK established when continuously on, and data transfer (activity) when blinking. If the lower green LED is permanently off, no LINK is established. The upper green/yellow dual-LED signals the link speed 1Gbit/s when lit yellow, 100Mbit/s when lit green, and 10Mbit/s when off. The RJ-45 LEDs remain in use, regardless of an optional port redirection to the rear I/O connector J2.

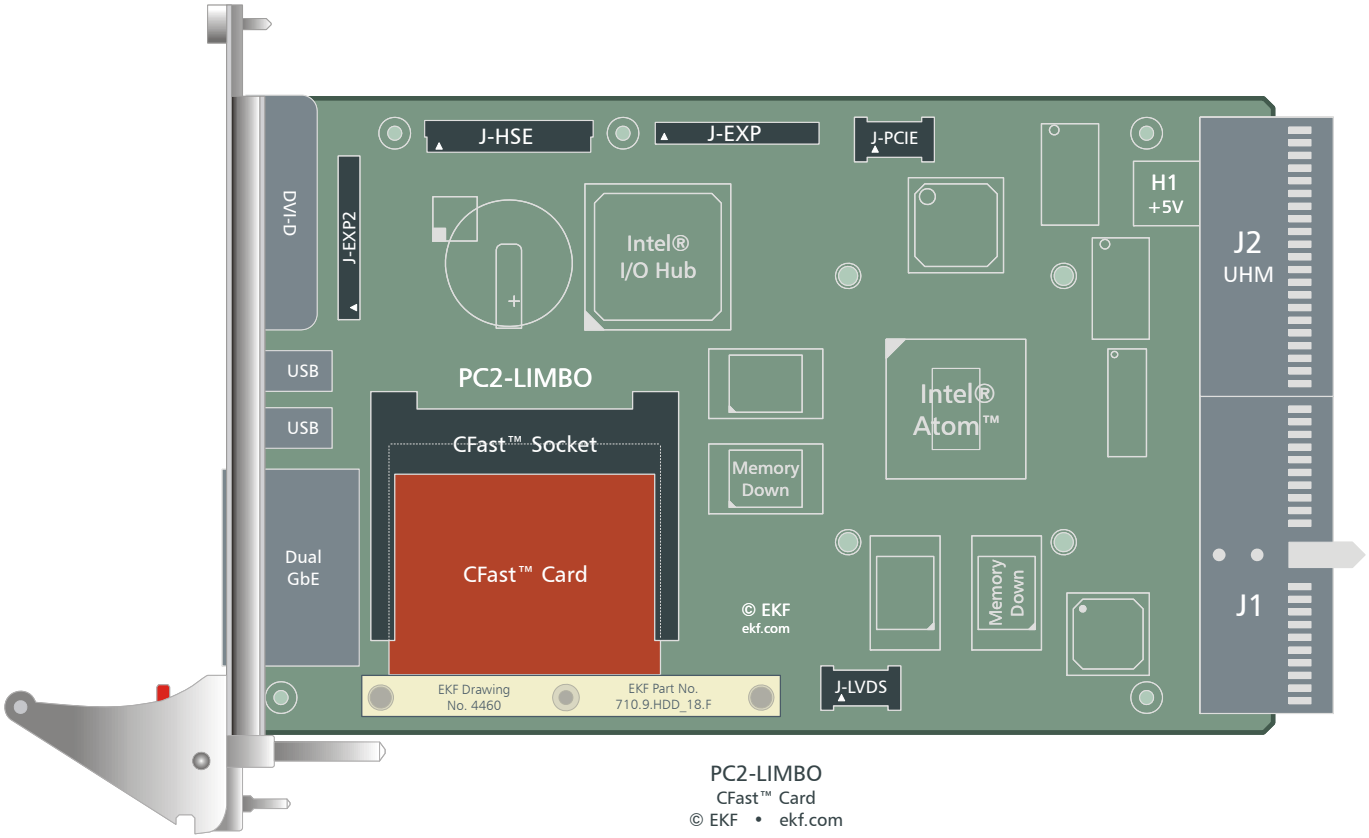
Mezzanine Connectors & Card Sockets

CFast™ Host Connector CF1

By default, the PC2-LIMBO is provided with a CFast™ host connector. It is suitable for CFast™ cards, which have the same dimensions as CompactFlash™ cards, but are operated in SATA mode. Industrial CFast™ SSD cards are available up to 64GB as of current. The SATA channel available on the CFast™ socket is derived directly from the Topcliff EG20T PCH. Since SATA based SSD modules are fast and reliable over the industrial temperature range, a CFast™ card can be used as boot device in many applications.

A guiding rail is provided to simplify card insertion. Once installed, the CFast™ card will have to be locked manually by a retainer latch (EKF part #218.5.024.29), in order to withstand shock and vibration. The latching part may be supplied loosely (not assembled on the PC2-LIMBO, depending on your order), and hence should be snapped onto the CFast™ socket first, before being used. When the PC2-LIMBO is combined with a low profile mezzanine module such as the C42-SATA, the latching retainer will be replaced by a mounting bar (EKF part #710.9.CFA.B).

There is some ambiguity about the top and bottom side of a CFast™ module - be sure to insert the card properly into the socket. For several CFast™ SSD card brands this would require the module to be inserted with its label facing downwards (to the PCB). However, leading suppliers (e.g. Swissbit) attach the label vice versa on their cards, which requires that such CFast™ modules have to be inserted with their label on top. Anyway, the finger grip, which is recessed into the cards end, should be up. Forced wrong insertion may cause permanent damage to the CFast™ card and the CFast™ host connector.

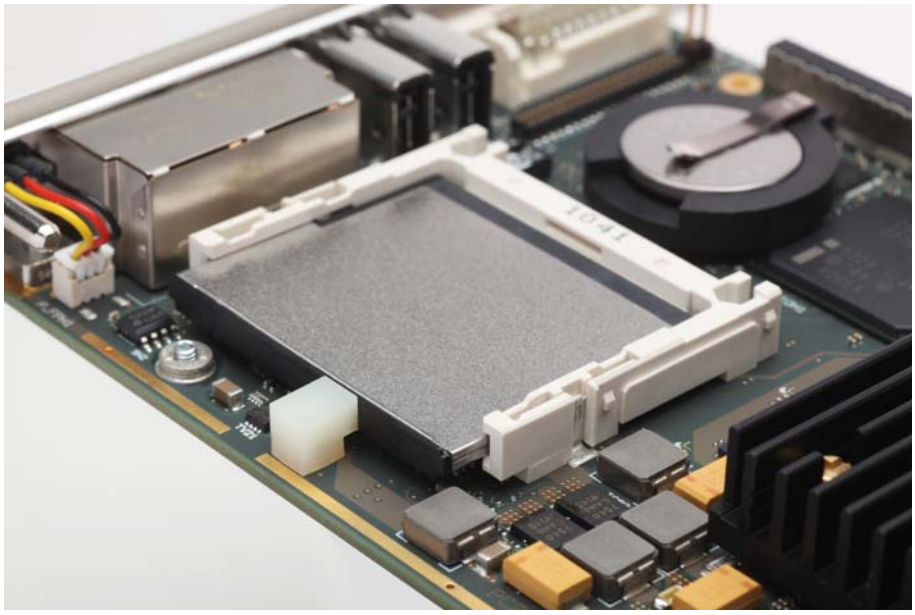


CFast Card Fixed by Mounting Bar (Padding Support for Mezzanines)

CF1 CFast™ Host Connector • 218.5.024.1	
Part No. 218.5.024.21 • CFast™ Host Connector  © EKF • ekf.com	
S1	GND
S2	SATA1_TXP
S3	SATA1_TXN
S4	GND
S5	SATA1_RXN
S6	SATA1_RXP
S7	GND
PC1	*CDI*
PC2	GND
PC3	*TBD*
PC4	*TBD*
PC5	*TBD*
PC6	*TBD*
PC7	GND
PC8	LED1 (PHYRDY Signal) 2)
PC9	LED2 (HDDA Signal) 2)
PC10	*IO1*
PC11	*IO2*
PC12	*IO3*
PC13	+3.3V 1)
PC14	+3.3V 1)
PC15	GND
PC16	GND
PC17	*CDO*

1) Overcurrent protected by 0.75A self resetting fuse. Alternate stuffing for +5V on request.
2) LED outputs not necessarily supported by a particular CFast™ card brand, routed to PC2-LIMBO on-board PLD

If the CFast™ host connector is not in use in an application, please remove the latching retainer assembly carefully from the socket (strut the snap-in clips on both sides). As an alternate, use an adhesive tape to fix the CFast™ retaining lever in its normal (locking) position. Otherwise, under worst conditions, the latching spring could cause a short circuit situation when unintentionally moving (forced by shock or vibration) and touching a PCB in the neighboured board slot of the system rack. From PCB Rev. 4 off, the CFast™ card is secured by a small retainer block (screw locked), as can be seen below.



Suitable CFast™ SSD Cards	
16GB, -40°C to +85°C	872.50.016.02
32GB, -40°C to +85°C	872.50.032.02
64GB, -40°C to +85°C	872.50.064.02

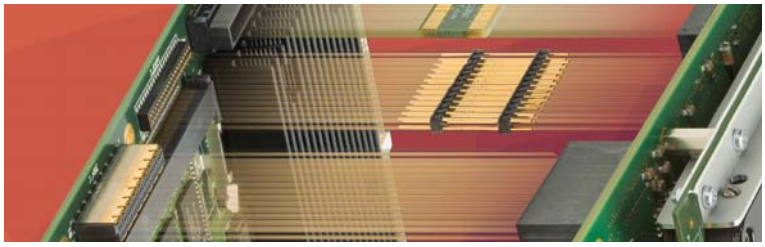
Known issue: Most CFast™ Cards (e.g. Delkin, Swissbit and other brands) work as expected. However, EKF had also cards under test which showed up strange behaviour. EKF therefore strongly recommends to validate thoroughly a chosen CFast™ card before ordering. If in doubt, please contact support@ekf.com.

Expansion Interface J-EXP(1)

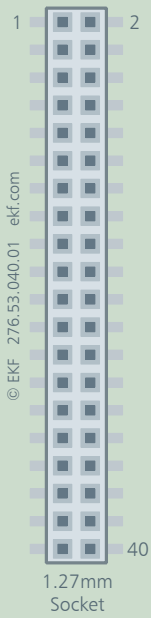
This connector conveys a variety of I/O signals, which are in use on several mezzanine side cards, such as the LPC (Low Pin Count) interface (required e.g. for a secondary SIO), the HD Audio (Azalia) port (connects to an audio codec), and the SMBus, all under control of the E6xx processor. Two USB ports are available in addition, which are derived directly from the Topcliff PCH.

J-EXP is referred here also as J-EXP1 in order to distinguish more clearly between J-EXP(1) and J-EXP2.

J-EXP



J-EXP (Exploded View)



J-EXP-T (J-EXP-B optinal)			
GND	1	2	+3.3V [1]
PCI_CLK (33MHz)	3	4	RST_PLC#
LPC_AD0	5	6	LPC_AD1
LPC_AD2	7	8	LPC_AD3
LPC_FRM#	9	10	100k PU *LPC_DRQ#*
GND	11	12	+3.3V [1]
LPC_SERIRQ	13	14	WAKE#
EXP_SMI#	15	16	SIO_CLK (14.3MHz)
NC	17	18	BKLTCTL (CPU GPIO_SUS2) [3]
KBRST#	19	20	BKLTEN (CPU GPIO_SUS1) [3]
GND	21	22	+5V [1]
USB_EXP2-	23	24	USB_EXP1-
USB_EXP2+	25	26	USB_EXP1+
USB_EXP_OC#	27	28	DBRESET#
EXP_SCL [2]	29	30	EXP_SDA [2]
GND	31	32	+5V [1]
HDA_SDOUT	33	34	HDA_SDIN0
HDA_RST#	35	36	HDA_SYNC
HDA_CLK	37	38	HDA_SDIN1
SPEAKER	39	40	VDDEN (CPU GPIO_SUS0) [3]

1) Power rail switched on in state S0 only
2) Connected to SMBus via buffered switch, isolated after reset
3) To be used in connection with J-LVDS

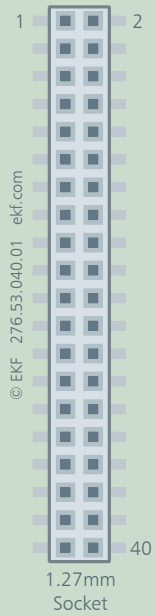
The expansion interface header footprint is available on both sides of the PC2-LIMBO, top (J-EXP-T) and bottom (J-EXP-B). The bottom side connector is stuffed only on customers request.

WARNING: Neither the +3.3V pins, nor the +5V pins are protected against a short circuit event. The connector J-EXP1 therefore should be used only for attachment of an approved expansion side card. The maximum current flow across these pins should be limited to <1A per power pin.

Expansion Interface J-EXP2

This connector conveys several I/O signal groups, for optional usage on a suitable mezzanine side card. These signals are comprised of a PS/2 mouse and keyboard port (derived from an on-Board SIO), and further a CAN interface, two UART channels, an I2C and a SDIO port (all derived from the EG20T Topcliff PCH). The CAN and UART lines on the J-EXP2 are 3.3V TTL-level based (UART pins are not 5V tolerant) and require external transceivers for attachment to ISO 11898 (CAN) or EIA-232/485 peripherals.

The connector J-EXP2 is not populated by default. Please contact sales@ekf.com for availability.



J-EXP2			
GND	1	2	+3.3V [1]
PS/2 MS_DAT	3	4	PS/2 KB_DAT
PS/2 MS_CLK	5	6	PS/2 KB_CLK
CAN_TX	7	8	I2C_CLK
CAN_RX	9	10	I2C_DAT
GND	11	12	+3.3V [1]
UART0_CTS	13	14	UART0_DCD
UART0_DSR	15	16	UART0_DTR
UART0_RI	17	18	UART0_RTS
UART0_RXD	19	20	UART0_TXD
GND	21	22	+5V [1]
UART1_RXD	23	24	UART1_TXD
SDIO1_PWR0	25	26	SDIO1_LED
SDIO1_WP [2]	27	28	SDIO1_CD# [2]
SDIO1_CLK	29	30	SDIO1_CMD
GND	31	32	+5V [1]
SDIO1_DATA0	33	34	SDIO1_DATA1
SDIO1_DATA2	35	36	SDIO1_DATA3
SDIO1_DATA4	37	38	SDIO1_DATA5
SDIO1_DATA6	39	40	SDIO1_DATA7

1) Power rail switched on in state S0 only
2) Terminated by resistors 10k P/U +3.3V

WARNING: Neither the +3.3V pins, nor the +5V pins are protected against a short circuit event. The connector J-EXP2 therefore should be used only for attachment of an approved expansion side card. The maximum current flow across these power pins should be limited to <1A per pin.

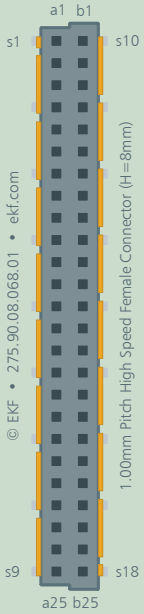
High Speed Expansion Connector J-HSE

Expansion Connector J-HSE and Low Profile Module

J-HSE can be used for attachment of a mezzanine card, either a small size low profile module, or an Eurocard size side board. Several low profile modules are available for on-board storage (CFast, Micro SATA, mSATA, CompactFlash, USB), in addition to the the CFast host connector provided on the PC2-LIMBO. Low profile modules fit into the 4HP profile of the carrier board, in contrast to side cards, which require at least 4HP system space in addition. The front panel width (8HP or even 12HP) for CPU board and side card is used for additional front I/O connectors, and most side cards can be equipped with a 2.5-inch SSD/HDD.

J-HSE Used for Side Card (8HP Assembly Unit)

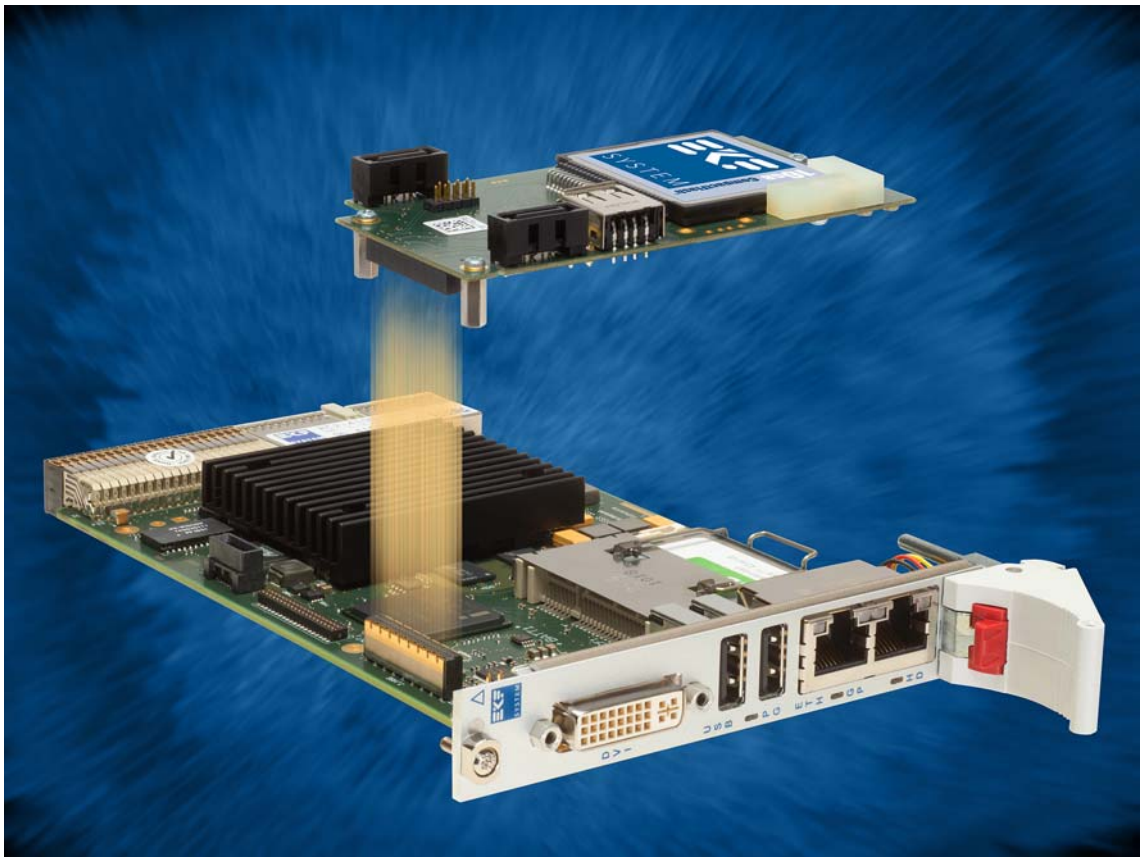
J-HSE is a high speed mezzanine connector, which conveys up to 3 x SATA channels and 4 x USB lines. The SATA channel 1 has been derived from the PCH, whereas the SATA channels 2 and 3 are connected to a JMB362 SATA RAID controller. The USB ports come from an 1:4 on-board USB hub.



High Speed Expansion J-HSE			
GND	a1	b1	GND
SATA_HSE1_TXP [3) 5)]	a2	b2	SATA_HSE3_TXP [4) 5) 6)]
SATA_HSE1_TXN [3) 5)]	a3	b3	SATA_HSE3_TXN [4) 5) 6)]
GND	a4	b4	GND
SATA_HSE1_RXN [3) 5)]	a5	b5	SATA_HSE3_RXN [4) 5) 6)]
SATA_HSE1_RXP [3) 5)]	a6	b6	SATA_HSE3_RXP [4) 5) 6)]
GND	a7	b7	GND
SATA_HSE2_TXP [4) 5) 6)]	a8	b8	
SATA_HSE2_TXN [4) 5) 6)]	a9	b9	
GND	a10	b10	GND
SATA_HSE2_RXN [4) 5) 6)]	a11	b11	
SATA_HSE2_RXP [4) 5) 6)]	a12	b12	
GND	a13	b13	GND
USB_HSE2_P	a14	b14	USB_HSE4_P
USB_HSE2_N	a15	b15	USB_HSE4_N
GND	a16	b16	GND
USB_HSE1_P	a17	b17	USB_HSE3_P
USB_HSE1_N	a18	b18	USB_HSE3_N
GND	a19	b19	GND
USB_HSE_OC#	a20	b20	USB_HSE_OC#
USB_HSE_OC#	a21	b21	USB_HSE_OC#
+3.3VS [1)]	a22	b22	+5VS [1)]
+3.3VS [1)]	a23	b23	+5VS [1)]
+3.3VA [2)]	a24	b24	+5VA [2)]
RSVD	a25	b25	*RSVD*

1) Power rail switched on in state S0 only (Switched)
2) Power rail on with system power (Always)
3) This SATA channel is derived from the PCH
4) These SATA channels are derived from a JMB362 dual-channel SATA RAID controller (option, not available with CPCI Classic versions of the PC2-LIMBO)
5) All TX/RX designations with respect to the SATA controller
6) SATA channels 2 and 3 not available concurrently with J2 Rear I/O - stuffing option on request

WARNING: The +3.3V/+5V power pins are not protected against a short circuit event. The connector J-HSE therefore should be used only for attachment of an approved expansion side card. The maximum current flow through these power pins should be limited to <0.5A per pin.



C40-CFA • CompactFlash Mezzanine Module

C41-CFAST • CFast Card Mezzanine

PC2-LIMBO w. C41-CFAST Low Profile Mezzanine Storage Module

C42-SATA • Solid State Drive Mezzanine Module

C43-SATA • Internal Connectors Mezzanine Module

PC2-LIMBO w. C43-SATA Low Profile Module

C44-SATA • 2.5-Inch HDD/SSD Carrier Side Card (8HP F/P Width)

C45-SATA • Front Panel Loading SSD Mezzanine Module (8HP F/P Width)

C47-MSATA • Low Profile RAID Storage Mezzanine Module

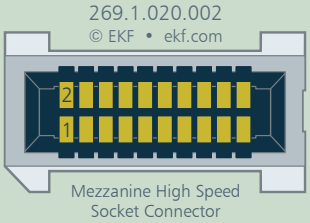
PC2-LIMBO w. C47-MSATA Mezzanine Storage Module (Option on Request)

RAID Option (on Request) with C47-MSATA Dual Mini Card SSD

Expansion Connector J-LVDS

The connector J-LVDS is only available as an option on request, for usage of the E6xx processor LVDS graphics port on a suitable future custom mezzanine card.

On a mezzanine card, the LVDS signals can be used for direct attachment of a suitable display, or can be converted into DVI, HDMI or VGA, as required. The LVDS graphics port is independent from the Tunnel Creek E6xx SDVO port (DVI), for a true dual-screen solution. Please contact sales@ekf.com for a customer specific mezzanine module according to your needs.



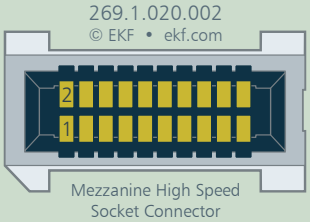
J-LVDS			
GND	1	2	GND
LVDS_DATA_P2	3	4	LVDS_DATA_P3
LVDS_DATA_N2	5	6	LVDS_DATA_N3
GND	7	8	GND
LVDS_DATA_P1	9	10	DDC_DAT (GPIO_SUS4)
LVDS_DATA_N1	11	12	DDC_CLK (GPIO_SUS3)
GND	13	14	GND
LVDS_DATA_P0	15	16	LVDS_CLK_P
LVDS_DATA_N0	17	18	LVDS_CLK_N
GND	19	20	GND

Please refer in addition to the J-EXP connector description, for the backlight and power control signals BKLTEN, BKLTCTL, and VDDEN.

PCI Express® Expansion Header J-PCIE

J-PCIE is a high speed connector, which is used widely for EKF side cards with PCI Expess® based I/O controllers. The PC2-LIMBO provides one PE link/lane (1x1) on this connector. Despite most EKF mezzanine side boards are wired as 1x4, they can be operated also from a single PE lane due to auto-negotiation, but there may exist also side cards which are not fully compatible with the PC2-LIMBO.

The PCIe lane is derived from a PE packet switch, which is provided on the CompactPCI® PlusIO versions of the PC2-LIMBO. For the CompactPCI® Classic versions of the PC2-LIMBO however, the PE packet switch is not populated, and the PCIe lane available on J-PCIE is derived directly from the Topcliff PCH.

J-PCIE				
	GND	1	2	GND
	+5V [1)]	3	4	+3.3V [1)]
	+5V [1)]	5	6	+3.3V [1)]
	GND	7	8	GND
	PE_CLKP	9	10	RST_PLC#
	PE_CLKN	11	12	PE_WAKE#
	GND	13	14	GND
	PE_1TP	15	16	PE_1RP
	PE_1TN	17	18	PE_1RN
	GND	19	20	GND

[1)] Power rail switched on in state S0 only

WARNING: The +3.3V/+5V power pins are not protected against a short circuit event. The connector J-PCIE therefore should be used only for attachment of an approved expansion side card. The maximum current flow through these power pins should be limited to <0.5A per pin.

J-PCIE Expansion Connector

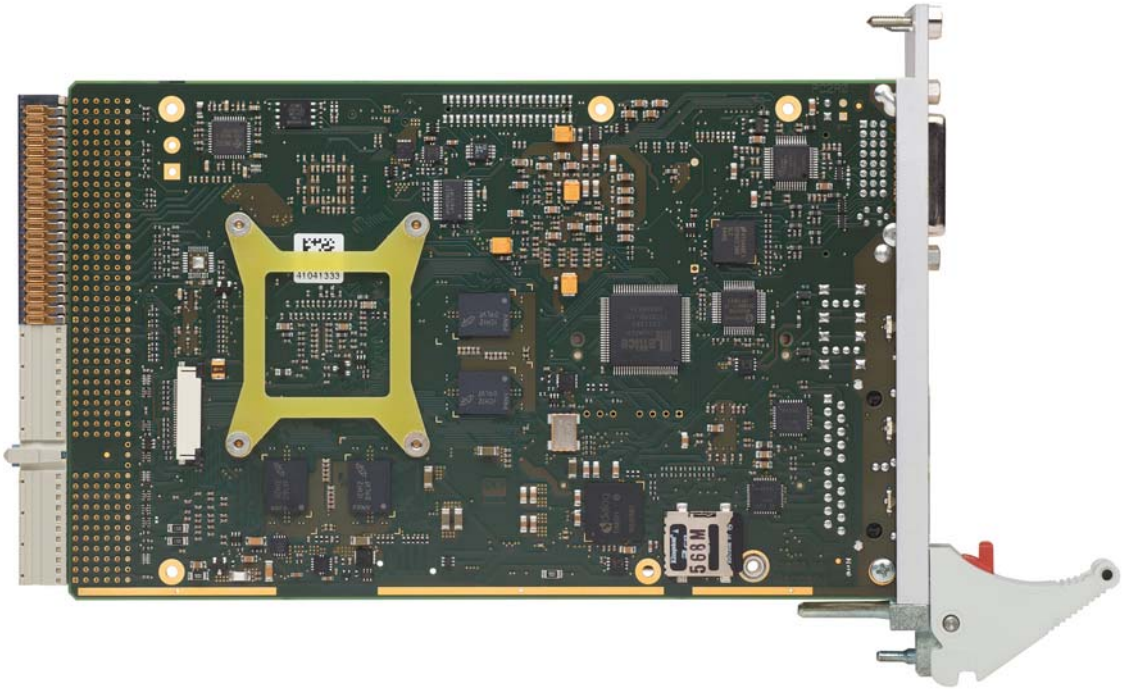
MSD1 microSD Card Holder

By default, the PC2-LIMBO is provided with a microSD card socket, located on the boards bottom side. MicroSDHC cards are available in several speed classes, which describe the minimum sustained data transfer rate. The PC2-LIMBO supports class 6 memory cards (6MB/s minimum read/write operation).
MicroSD and microSDHC cards are available for the extended or industrial temperature range, with a capacity of up to 32GB as of current. Industrial grade microSDHC memory cards can be ordered as accessory with the PC2-LIMBO.

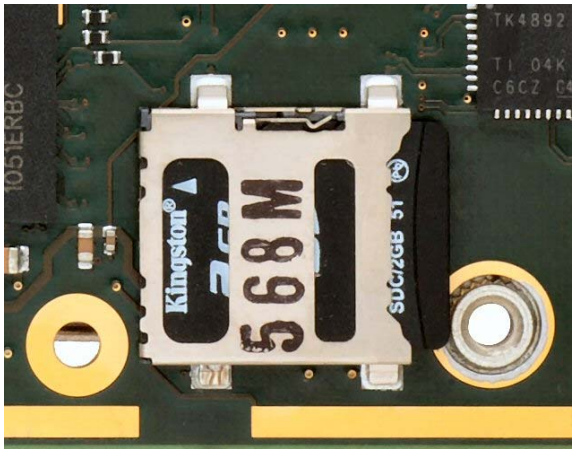
Insert the microSDHC card carefully into the holder (card contacts facing downwards to the PCB, card labelling visible when inserting, observe also the arrow marking). Forced wrong insertion may cause permanent damage to the microSD card and the host connector. The microSDHC card can be fixed by a short M2.5 screw (threaded PCB insert provided adjacent to the card)..

microSDHC Host Connector • 218.6.008.1	
218.6.008.1 • microSD Card Holder © EKF • ekf.com 	
1	DAT2
2	DAT3
3	CMD
4	+3.3V
5	CLK
6	GND
7	DAT0
8	DAT1

Suitable microSDHC Flash Memory Cards	
8GB, speed class 6, -25°C to +85°C	888.1.006.0008.00
16GB, speed class 6, -25°C to +85°C	888.1.006.0016.00



PC2-LIMBO Bottom View (Card Holder Near F/P Handle)



Threaded Insert

Pin Headers & Debug

Front Panel Handle Microswitch Header P-FPH

The jumper P-FPH is used for attachment of an external SPDT switch. By default, P-FPH is connected across a short cable harness to a microswitch, which is integrated into the PC2-LIMBO front panel handle (ejector lever). The switch performs a power button event (e.g. system shutdown) by short-circuiting the pins 1 and 3 of P-FPH when activated (hold unlock button of front panel handle depressed momentarily).

P-FPH		
# 276.02.003.11 © EKF • ekf.com 		
1	black	Microswitch Pole (Common), Wired to PLD
2	red	Microswitch Throw - F/P Handle Locked Position, NC
3	yellow	Microswitch Throw - F/P Handle Unlocked Position, Wired to GND

PLD Programming Header P-ISP

The PC2-LIMBO is provided with a powerful PLD (in-System Programmable Logic Device) which replaces legacy glue logic. The programming header P-ISP is normally not stuffed (in use for manufacturing only). Its footprint is situated at the bottom side of the board.

P-ISP	
240.1.08.I • © EKF • ekf.com 	
1	+3.3V
2	TDO
3	TDI
4	*NC*
5	*KEY*
6	TMS
7	GND
8	TCK

Processor Debug Header XDP1

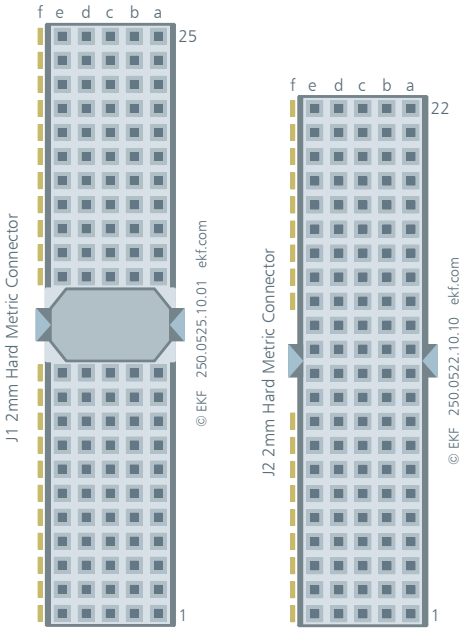
The PC2-LIMBO may be equipped with a 26-position processor debug header for hard- and software debugging (specified by Intel® as XDP-SFF-26 Pin Platform Connection). The connector is suitable for installation of a flat flex cable (FFC), in order to attach an JTAG debugger (emulator) such as the Arium ECM-XDP3. An adapter (ITP-XDP-SFF-26) is required in addition to convert the 26-pin XDP-SFF-26 Pin connector to the standard 60-pin XDP.

The header XDP1 would be mounted on the PCB bottom side, but is not stuffed by default.

XDP Processor Debug Connector • 269.1.026.902	
269.1.026.902 • FFC Connector  © EKF • ekf.com	
1	OBSFN_A0 (PREQ#)
2	OBSFN_A1 (PRDY#)
3	GND
4	OBSDATA_A0 (BPM3)
5	OBSDATA_A1 (BPM2)
6	GND
7	OBSDATA_A2 (BPM1)
8	OBSDATA_A3 (BPM0)
9	GND
10	HOOK0 (PWRMODE0)
11	HOOK1 (PWRMODE1)
12	HOOK2 (PWRMODE2)
13	*HOOK3*
14	HOOK4 (BCLKP)
15	HOOK5 (BCLKN)
16	VCCOBS_AB (+1.05V)
17	HOOK6 (CPU_RST#)
18	HOOK7 (DBRESET#)
19	GND
20	TDO
21	TRST#
22	TDI
23	TMS
24	*TCK1*
25	GND
26	TCK0 (TCK)

Backplane Connectors

Two hard metric backplane connectors are specified as J1/P1 and J2/P2 by the PICMG® CompactPCI 2.0 and 2.30 (PlusIO). J1 conveys the 32-bit PCI parallel bus, and J2 provides primarily the Rear I/O signals defined by the PlusIO specification.



J2 is a high speed UHM connector, suitable for Gigabit Serial I/O as defined by the PICMG® 2.30 CompactPCI® PlusIO Specification. This specification defines the I/O assignment of the J2/P2 32-bit CompactPCI® System Slot connector in order to extend the parallel PCI bus with high-speed serial busses. CompactPCI® PlusIO defines the support of PCI, PCI Express, Ethernet, SATA/SAS and USB concurrently. In addition to the parallel PCI bus architecture this I/O specification allows the use of the CompactPCI® system slot to provide a simple star architecture based on the specified serial bus standards. The PlusIO definition is fully backward compatible to 32-bit CompactPCI® and will interoperate with existing 32-bit systems. This standard allows the implementation of hybrid backplanes: CompactPCI® with CompactPCI® Express and/or CompactPCI® Serial. A 32-bit CompactPCI® PlusIO System can be used as a system slot for CompactPCI® Serial or CompactPCI® Express as well.

J2 UHM (Top)
J1 (Bottom)

CompactPCI® Backplane Connector J1

J1	A	B	C	D	E
25	5V	*REQ64#* [2]	ENUM# [1]	3.3V	5V
24	AD1	5V	V(I/O)	AD0	*ACK64#* [2]
23	3.3V	AD4	AD3	5V	AD2
22	AD7	GND	3.3V	AD6	AD5
21	3.3V	AD9	AD8	GND/M66EN [3]	C/BE0#
20	AD12	GND	V(I/O)	AD11	AD10
19	3.3V	AD15	AD14	GND	AD13
18	SERR# [1]	GND	3.3V	PAR	C/BE1#
17	3.3V	IPMB SCL [4]	IPMB SDA [4]	GND	PERR# [1]
16	DEVSEL# [1]	GND	V(I/O)	STOP# [1]	LOCK# [1]
15	3.3V	FRAME# [1]	IRDY# [1]	BD_SEL# [7]	TRDY# [1]
14	KEY AREA				
13					
12					
11	AD18	AD17	AD16	GND	C/BE2#
10	AD21	GND	3.3V	AD20	AD19
9	C/BE3#	GND	AD23	GND	AD22
8	AD26	GND	V(I/O)	AD25	AD24
7	AD30	AD29	AD28	GND	AD27
6	REQ# [1]	GND	3.3V	CLK	AD31
5	*BRSVP1A5* [5]	*BRSVP1B5* [5]	RST#	GND	GNT0#
4	IPMB PWR	GND	V(I/O)	INTP [1]	INTS [1]
3	INTA# [1]	INTB# [1]	INTC# [1]	5V	INTD# [1]
2	*TCK* [5]	5V	*TMS* [5]	*TDO* [5]	*TDI* [5]
1	5V	-12V [6]	*TRST#* [5]	+12V	5V

1) 1k PU resistor to V(I/O), other PU values (e.g. 2.7k for V(I/O)=+3.3V) available on request
2) Not used on PC2-LIMBO, but has 1k PU to V(I/O), other PU values on request
3) 4.99k PU by default, can be optionally fixed to GND to force 33MHz operation (0R PD)
4) 3.0k PU to J1 pin A4 IPMBPWR
5) Not connected
6) Connected to a decoupling capacitor, not used on PC2-LIMBO
7) Input connected to on-board power sequencing logic, driven low by an external hot swap controller to enable power on, or permanently pulled low on the backplane

The PC2-LIMBO has been designed for +5V only operation. The board can feed +3.3V to the backplane (please refer to chapter '+5V Only Design' for details).

CompactPCI® Backplane Connector J2 (PlusIO)

The PC2-LIMBO can provide up to 2 x GbE, 4 x PCIe, 4 x SATA and 4 x USB for rear I/O across J2. The Gigabit Ethernet rear I/O ports are shared with the front panel jacks (setup redirection via BIOS). The PE lanes are derived from an on-board PE switch (4 links by 1 lane each). With respect to SATA, the channels 3/4 are available either via J2 (stuffing option on request only), or through the mezzanine connector J-HSE (default). SATA 1/2 and SATA 3/4 each have their own dual-port SATA controller (software RAID capable). The rear I/O USB ports are generated from an on-board 1:4 USB hub.

On CompactPCI® Classic versions of the PC2-LIMBO all components wired for RIO have been removed, and the UHM J2 connector will be replaced by a normal HM connector.Please note, that open PCB copper traces to J2 are still existent, which may downgrade the P2 backplane signal quality (stubs).

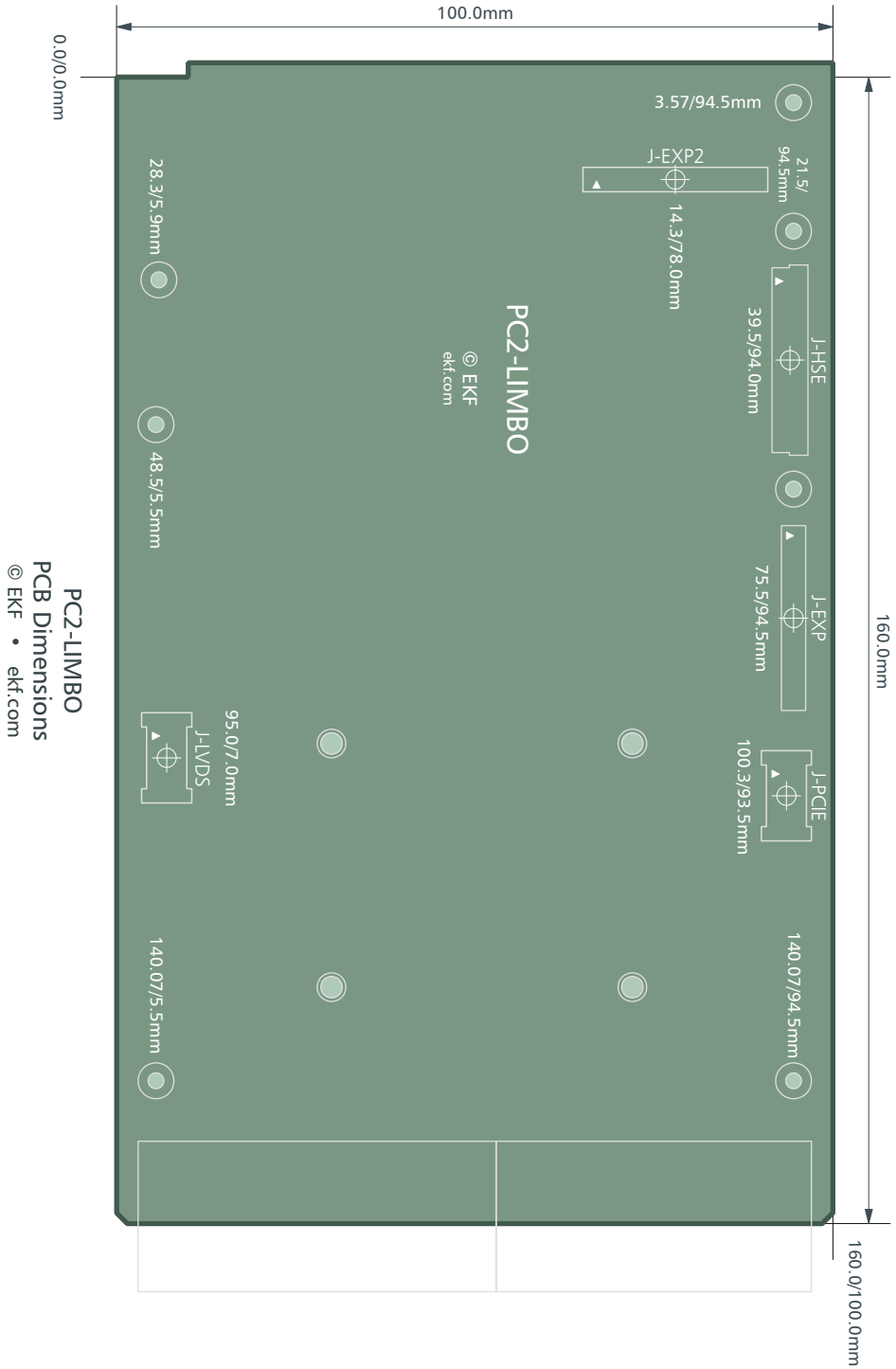
J2	A	B	C	D	E
22	*GA4* [2]	*GA3* [2]	*GA2* [2]	*GA1* [2]	*GA0* [2]
21	CLK6	GND	2_ETH_B+	1_ETH_D+	1_ETH_B+
20	CLK5	GND	2_ETH_B-	1_ETH_D-	1_ETH_B-
19	GND	GND	2_ETH_A+	1_ETH_C+	1_ETH_A+
18	2_ETH_D+	2_ETH_C+	2_ETH_A-	1_ETH_C-	1_ETH_A-
17	2_ETH_D-	2_ETH_C-	PRST# [1]	REQ6# [1]	GNT6#
16	4_PE_CLK-	2_PE_CLK+	DEG# [1]	GND	reserved [2]
15	4_PE_CLK+	2_PE_CLK-	FAL# [1]	REQ5# [1]	GNT5#
14	3_PE_CLK-	1_PE_CLK+	4_PE_CLKE#	*SATA_SCL* [2]	reserved [2]
13	3_PE_CLK+	1_PE_CLK-	3_PE_CLKE#	*SATA_SDO* [2]	*SATA_SL* [2]
12	4_PE_RX00+	1_PE_CLKE#	2_PE_CLKE#	*SATA_SDI* [2]	4_SATA_RX+ [4]
11	4_PE_RX00-	4_PE_TX00+	4_USB2+	4_SATA_TX+ [4]	4_SATA_RX- [4]
10	3_PE_RX00+	4_PE_TX00-	4_USB2-	4_SATA_TX- [4]	3_SATA_RX+ [4]
9	3_PE_RX00-	3_PE_TX00+	3_USB2+	3_SATA_TX+ [4]	3_SATA_RX- [4]
8	2_PE_RX00+	3_PE_TX00-	3_USB2-	3_SATA_TX- [4]	2_SATA_RX+
7	2_PE_RX00-	2_PE_TX00+	2_USB2+	2_SATA_TX+	2_SATA_RX-
6	1_PE_RX00+	2_PE_TX00-	2_USB2-	2_SATA_TX-	1_SATA_RX+
5	1_PE_RX00-	1_PE_TX00+	1_USB2+	1_SATA_TX+	1_SATA_RX-
4	V(I/O)	1_PE_TX00-	1_USB2-	1_SATA_TX-	reserved [2]
3	CLK4	GND	GNT3#	REQ4# [1]	GNT4#
2	CLK2	CLK3	SYSEN# [3]	GNT2#	REQ3# [1]
1	CLK1	GND	REQ1# [1]	GNT1#	REQ2# [1]

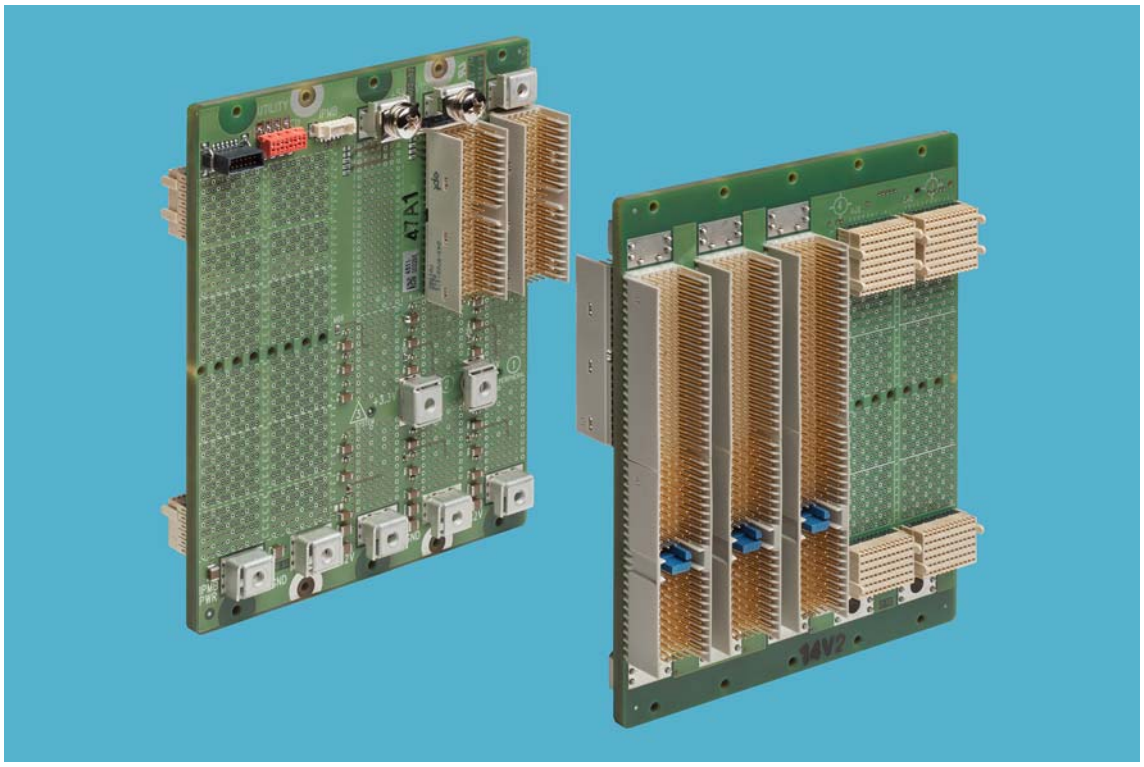
1) PU 1k to V(I/O), alternate pull up values (e.g. 2.7k for V(I/O)=+3.3V) available on request
2) Not connected
3) PU 10k to +3.3V
4) SATA 3/4 on J2 not available concurrently to J-HSE, stuffing option on customer request

Appendix

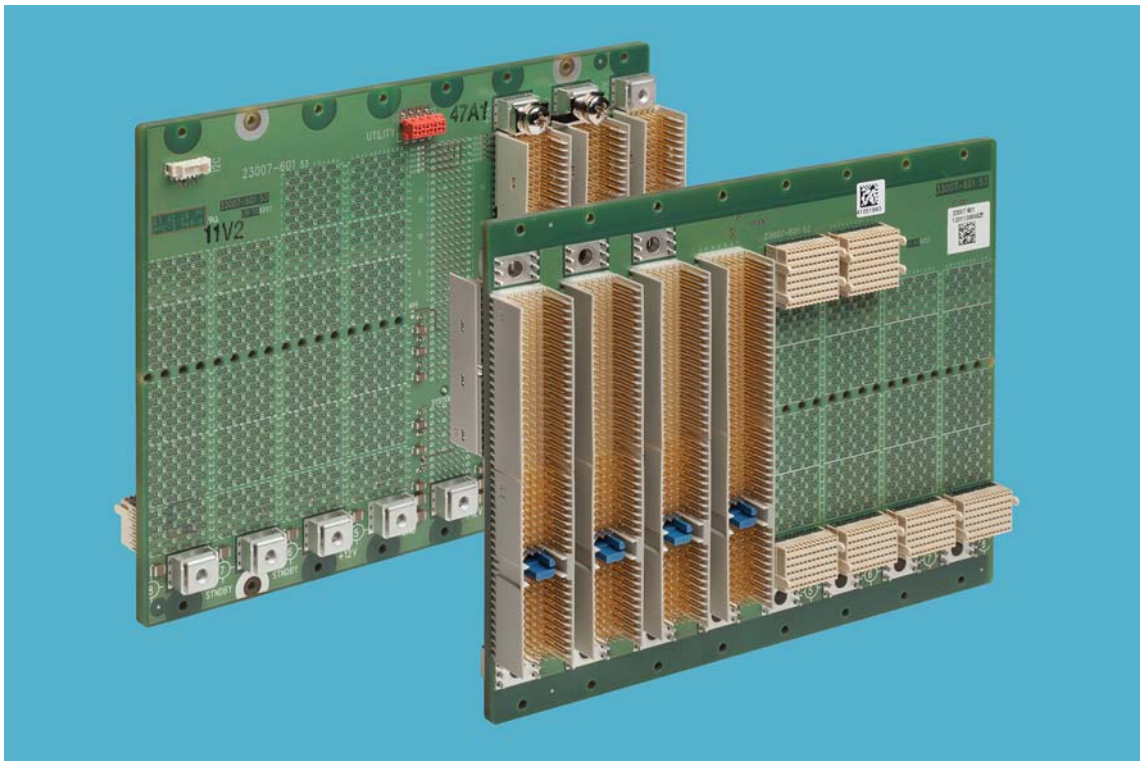
Mechanical Drawing

The following drawing shows the positions of mounting holes and expansion connectors on the PC2-LIMBO.





Sample Hybrid Backplane 3 + 2 Slots



Sample Hybrid Backplane 4 + 4 Slots

Industrial Computers Made in Germany

boards. systems. solutions.

EKF Elektronik GmbH
Philipp-Reis-Str. 4 (Haus 1)
Lilienthalstr. 2 (Haus 2)
59065 HAMM
Germany

Phone +49 (0)2381/6890-0
Fax +49 (0)2381/6890-90
Internet www.ekf.com
E-Mail sales@ekf.com